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CAMAC 577 -- Timer Module

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General Description

The CAMAC 577 MODULE provides eight timing channels. Each channel is composed of a 32-bit counter which is normally clocked by a 1MHz signal derived from the Tevatron clock (TCLK). Timing cycles are normally triggered by events encoded on the TCLK. TCLK events can be qualified by machine states, based on MDAT data. Each channel may be programmed independently with respect to delay, clock events, and machine state.

The programmable channel delay may range from a minimum of 2usec to a max of FFFF FFFFH microseconds (approx. 1.2 Hrs). These delays are based on the 10 MHz TCLK carrier. A RAM is used on the module as the storage medium for counter presets. When a TCLK event trigger occurs, the counter preset is loaded from RAM.

The clock events to be used as triggers are selectable and may include any of the possible 256 events. A maximum of fifteen events are allowed per channel, per machine state. A RAM is used on the module as the storage medium for events.

The machine states to be used to qualify TCLK events are selectable and may include any of the 256 possible MDAT TypeCodes, and any of the 2^16 possible Data values for each TypeCode. A maximum of 15 machine state qualifiers are allowed per channel. Each programmed machine state will have its own counter preset and TCLK trigger table. A RAM is used on the module as the storage medium for machine states. A machine state and its associated counter preset and TCLK trigger table are selected for programming by setting the Machine State Pointer to 1-15.

An additional counter preset and TCLK trigger table are available per channel (Machine State Pointer = 0), which allow the user to define card behavior when:

1. No MDAT machine state match is detected
2. No MDAT signal is available
3. Qualification of TCLK events with machine state is not desired

CAMAC writes to the delay presets may happen at any time and will not interfere with counter operation. Data written to the delay preset of a busy counter will not take effect until the counter is done.

CAMAC writes to the TCLK trigger tables may happen at any time and will not interfere with counter operation.

CAMAC writes to the MDAT machine state registers may happen at any time and will not interfere with counter operation.

The eight channels may be enabled or inhibited separately or as a group. The channel's status word contains an enable/inhibit status bit. However, with the exception of the initial enable command, the enable/inhibit commands are not normally used in this module. Since the module will internally inhibit and enable channels for new settings, they need not be executed by the front

end (for purposes of new settings). This decreases front end burden and allows the externally written inhibit command to be used as a panic button to stop a channel even if it is busy. Enabling a previously inhibited, loaded channel will cause the channel to be reloaded and to wait for a trigger.

Provisions are made for an external clock and an external clock trigger. These are to be used together as an alternative to the TCLK. The maximum frequency of the external clock is 10 MHz. If the external clock frequency is less than 10MHz, the delay time must be scaled accordingly. A jumper header is provided to allow selected channels to respond to the external trigger signal. If one of the programmed Machine States is active, the counter preset associated with that state will be loaded into the counter. If none of the programmed Machine States is active, the counter preset associated with Machine State 0 will be loaded. Either an external trigger or a Tevatron event may be used for a channel trigger but they may not be OR'ed.

Module LAM is generated only upon absence of clock signal, either TCLK or external. LAM (clock) status is readable by means of each channel's status word.

This module is provided with an EEPROM which allows the return of operation after a power down. After power up, EEPROM data is tested for validity and, if valid, is used to load counters, set event triggers, and enable channels as they were configured prior to power down. One must allow at least 15 seconds after changing any setting to guarantee that the new setting is stored to EEPROM, before powering down or resetting the module.

The eight outputs each provide a positive 3 volt 1usec pulse upon timeout. Each has a series output diode to make possible external OR'ing of channels. If external OR'ing is necessary, care should be taken to keep the output cables as short as possible because long runs can produce transmission line mismatch effects.

OPCODES

Counter Preset, Channel N

This command will return the counter preset for Channel N and Machine State M, where M is the value of the Machine State Pointer, set by F(19).

F(0) A(N) – Read channel counter value -- low word

Bits	Bit Definitions
R16:R1	Low Preset Value C15:C0

F(1) A(N) – Read channel counter value -- high word

Bits	Bit Definitions
R16:R1	High Preset Value C31:C16

Read Machine State for Channel N

This command will return Machine State M for Channel N, where M is the value of the Machine State Pointer, set by F(19).

The current value of the Machine State Pointer is also included in this read.

Note: MDAT TypeCode and Data are valid only for Machine State Pointer = 1-15. MDAT TypeCode and Data programmed for Machine State Pointer = 0 will be ignored by the C577. As such, data returned with F(2) and F(3) for MSP = 0 is meaningless and should be disregarded.

F(2) A(N) – Read Machine State Pointer and MDAT TypeCode

Bits	Bit Definitions
R16:R13	Unused (read as zeros)
R12:R9	Machine State Pointer
R8:R1	Machine State MDAT TypeCode

F(3) A(N) – Read Machine State MDAT Data

Bits	Bit Definitions
R16:R1	Machine State MDAT Data

Read TCLK Trigger Table for Channel N, Auto Increment

This command returns data from the TCLK Trigger Table for Channel N and Machine State M, where M is the value of the Machine State Pointer, set by F(19).

This command will return two bytes per read. The pointer will be initialized by any opcode. Q will be delayed on the first read only. Thereafter, X and Q are returned immediately along with data.

If more than fifteen events are written to a channel, they will not be stored. Also if reads beyond the event count are executed, the last byte read will be repeated.

F(4) A(N) – Read events, auto increment

Word	Bits	Bit Definitions
1	R8:R1	Event Count
	R16:R9	Event 1
2	R8:R1	Event 2
	R16:R9	Event 3
3	R8:R1	Event 4
	R16:R9	Event 5
4	R8:R1	Event 6
	R16:R9	Event 7
5	R8:R1	Event 8
	R16:R9	Event 9
6	R8:R1	Event 10
	R16:R9	Event 11
7	R8:R1	Event 12
	R16:R9	Event 13
8	R8:R1	Event 14
	R16:R9	Event 15

Read Software Version

F(5) A(0) – Read Software Version

Bits	Bit Definitions
R16:R1	Software Version

Read Module Number

F(6) A(0) – Read Module Number

Bits	Bit Definitions
R16:R1	Hard Coded to 0x0241 (577d)

Read Channel N Status

F(7) A(N) – Read Channel Status

Bits	Bit Definitions
R16:R5	Unused. Hard-coded to 0x000
R4	S3 = 1 if the channel's counter is busy
R3	S2 = 0 (Unused)
R2	S1 = 1 if clock is present (LAM)
R1	S0 = 1 if channel is enabled

F(9) A(0) – Reset Module

A module reset will:

- Perform reset as does Z*S2 and power up clear.
- Do a RAM and EEPROM Data validation.
- Initialize all RAM and all counters to 00.
- Re-establish previous enable conditions, trigger events, and counter settings.

The reset operation should be allowed 1 second to complete.

All data, W or R, are don't-cares for this function.

F(9) A(1) – Reset Module with EEPROM Initialization

Leaves all channels inhibited and all counter values set to 0.

All data, W or R, are don't-cares for this function.

Write Channel N Counter Value

Note: The module will accept any value from 0x0000_0000 to 0xFFFF_FFFF as a counter value. However, the minimum delay the module can produce is 2 microseconds. Writing 0 or 1 as a delay will yield a delay of 0xFFFF_FFFF microseconds.

F(16) and F(17) must be used together whenever setting a counter preset. The 32-bit counter preset will be stored when F(17) is invoked, provided that F(16) immediately preceded F(17). Invoking F(17) before the lower 16 bits of the preset have been defined with F(16) is invalid and will be ignored, even though Q may be returned.

F(16) A(N) – Write Channel Counter Value, Low Word

Bits	Bit Definitions
W16:W1	Low Counter Value C15:C0

F(17) A(N) – Write Channel Counter Value, High Word

Bits	Bit Definitions
W16:W1	High Counter Value C31:C16

Write TCLK Trigger Table for Channel N

The event number may range from 00 to FF and once written to a specified channel, will trigger that channel upon receiving the event via the Tevatron clock. Fifteen events may be written for each value of the Machine State Pointer. If greater than fifteen are written, the excess will be ignored. Also repeat writing of an event will not result in duplicate entries.

Note: Define a TCLK Trigger Table for Machine State Pointer = 0 to define behavior when:
1. No MDAT signal is available
2. No MDAT machine state match is detected
3. Qualification of TCLK events with machine state is not desired

Note: Using the Delete All Events command will erase the TCLK Trigger Table for this Machine State Pointer, effectively disabling the Machine State defined with F(20) and F(21).

Note: Use the Delete All Events command with Machine State Pointer = 0 to disable all triggering for Channel N when:
1. No MDAT signal is available
2. No MDAT machine state match is detected

F(18) A(N) – Write Event Number and Control Byte for Channel N

Bits	Bit Definitions
W16:W11	Unused
W10:W9	1x: Delete all events 01: Delete Single Event 00: Add Event
W8:W1	Event Number

Write Machine State Pointer

The Machine State Pointer determines which Machine State MDAT TypeCode/Data, Counter Preset, and TCLK Trigger Table are being read and written.

Note: MDAT TypeCode and Data are ignored by the C577 for Machine State Pointer = 0. Machine State Pointer = 0 should be used to define behavior when:
1. No MDAT signal is available
2. No MDAT machine state match is detected
3. Qualification of TCLK events with machine state is not desired

Note: The CAMAC bus master must wait 100 msec after writing the Machine State Pointer before again attempting to access the C577.

F(19) A(0) – Write Machine State Pointer

Bits	Bit Definitions
W16:W5	Unused
W4:W1	Machine State Pointer

Write Machine State to Channel N

A Machine State is defined with an MDAT TypeCode/Data Value pair. The TypeCode number may range from 00 to FF. The Data Value may range from 0000 to FFFF.

Channel N will ignore all Tevatron Clock events unless one of the following is true:
1. One of the defined Machine States matches most recently received MDAT Data (group of MDAT data received between TCLK $07 events).
2. A TCLK Trigger Table has been defined for Machine State Pointer = 0

Multiple entries may be used for a given MDAT Typecode, allowing multiple MDAT Data values to be entered for a given TypeCode.

F(20) and F(21) must be used together whenever defining or modifying Machine State MDAT TypeCode/Data pairs. The Machine State MDAT TypeCode value entered with F(20) will be stored when F(21) is invoked. Invoking F(21) before an MDAT TypeCode value has been defined with F(20) is invalid and will be ignored, even though Q may be returned.

F(20) A(N) – Write MDAT TypeCode

Bits	Bit Definitions
W16:W9	Unused
W8:W1	Machine State: MDAT TypeCode

F(21) A(N) – Define MDAT Data Value and store MDAT Data Value

Bits	Bit Definitions
W16:W1	Machine State: MDAT Data Value

Channel Inhibit / Enable

F(24) A(N) – Inhibit Channel N

F(26) A(N) – Enable Channel N

F(28) A(0) – Inhibit all channels

F(30) A(0) – Enable all channels

Notes:

- Inhibit / Enable status is read by status read F(7) A(N).
- A channel will reload if inhibited and enabled.
- All data, W or R, are don't-cares for the Inhibit / Enable functions.

CAMAC 577 MODULE OPCODE SUMMARY

F(0) A(N) – Read channel N counter preset - low word

F(1) A(N) – Read channel N counter preset - high word

F(2) A(N) – Read Machine State Pointer and MDAT TypeCode

F(3) A(N) – Read Machine State MDAT Data Value

F(4) A(N) – Read TCLK Trigger Table for channel N

F(5) A(0) – Read software version number

F(6) A(0) – Read module number

F(7) A(N) – Read channel N status

F(9) A(0) – Reset module, restore settings

F(9) A(1) – Reset module, clear settings

F(16) A(N) – Write channel N counter value - low word

F(17) A(N) – Write channel N counter value - high word

F(18) A(N) – Write event number and control byte for channel N

F(19) A(0) – Set Machine State Pointer

F(20) A(N) – Write Machine State (TypeCode) and control byte for channel N

F(21) A(N) – Write Machine State (Data Value) for channel N [latched by F(23) A(N)]

F(24) A(N) – Inhibit channel N

F(26) A(N) – Enable channel N

F(28) A(0) – Inhibit all channels

F(30) A(0) – Enable all channels

Processor I/O Memory Map

There are two identical FPGAs on the Camac 577 board. Each FPGA controls activity for four counter channels (0 thru 3 and 4 thru 7). The I/O memory map for each FPGA is identical. An FPGA is selected when the processor asserts CS0 or CS1.

Because the two FPGAs are identical, they both contain a CAMAC bus interface. Only FPGA0 (selected with CS0) is used to communicate with CAMAC. The CAMAC interface of FPGA1 is not connected to the CAMAC bus or any processor interrupt.

Address	Register Definition
0x0000	Busy Status (Read Only)
0x0001	Counter Clock Present Status (Read Only)
0x0002 – 0x07FF	Reserved
0x0800 – 0x0FFF	TCLK Event Definitions
0x1000 – 0x10FF	MDAT Machine State Definitions
0x1100 – 0x17FF	Reserved
0x1800 – 0x18FF	Counter Presets
0x1900 – 0x1FFF	Reserved
0x2000	Channel Enables
0x2001 – 0x27FF	Reserved
0x2800	Heartbeat Strobe
0x2801	Counter Module Reset
0x2802 – 0x2FFF	Reserved
0x3000 – 0x3006	CAMAC Interface
0x3007 – 0x3FFF	Reserved

0x0000 – Busy Status Register

Bits	Bit Definitions	Value at Reset
7:0	Bit N = 1 indicates that Channel N has been triggered and is counting.	0x00

0x0001 – Counter Clock Present Status Register

Bits	Bit Definitions	Value at Reset
7:2	Unused These bits are unused and will read as zeros	0x00
1	1 = MDAT is present	0b
0	1 = Clock is present Clock can be either TCLK Carrier or External Clock	0b

0x0800 : 0x0FFF – TCLK Trigger Tables

This address space is broken up as follows:

ADDR[13:0] = 00_1NNT_TTTT_TTTB, where:

NN = Lower two bits of channel number (0 thru 3 or 4 thru 7)

TTTTTTTT = TCLK Event select

B = High/Low byte select:
0 for Machine State Pointer 0-7
1 for Machine State Pointer 8-15

Writing a 1 to bit M of the 16-bit word (high/low byte selected by B) enables TCLK event TTTTTTTT to trigger channel NNN when the MDAT TypeCode/Data pair defined by Machine State M is present.

For example, if we want to trigger on TCLK $10 when Machine State 14 for active for Channel 3, then:
NN = 11
TTTTTTTT = 00010000 ($10)
B = 1
We write 0x40 to address 0x0E21.

Bits	Bit Definitions	Value at Reset
7:0	TCLK Trigger Table Data	Uninitialized

Note: With the processor running at 8 MHz, the RDn line must be asserted for at least 3 clocks to guarantee valid data when reading from the TCLK Trigger Table area.

0x1000 : 0x10FF – MDAT Machine State Definitions

This address space is broken up as follows:

ADDR[13:0] = 01_0000_NNSS_SSBB, where:

NN = Lower two bits of channel number (0 thru 3 or 4 thru 7)
SSSS = MDAT Machine State Select (1 thru 15)
BB = Byte offset. Data elements are described below

BB = 00 – MDAT TypeCode

Bits	Bit Definitions	Value at Reset
7:0	MDAT TypeCode for Entry SSSS	Uninitialized

BB = 01 – MDAT Data (LSB)

Bits	Bit Definitions	Value at Reset
7:0	MDAT Data for Entry SSSS, Least Significant Byte	Uninitialized

BB = 10 – MDAT Data (MSB)

Bits	Bit Definitions	Value at Reset
7:0	MDAT Data for Entry SSSS, Most Significant Byte	Uninitialized

BB = 11 – Unused

Bits	Bit Definitions	Value at Reset
7:0	These bits are unused and will be ignored by the FPGA logic	Uninitialized

Data bytes must be written in groups of three bytes. Data for a 24-bit word is captured with the write to the high byte (BB = 10).

Note: Running at 8 MHz, the processor must wait at least 3 clocks after writing to BB = 10, to guarantee all data is captured by the FPGA, before performing another write operation to the MDAT Machine State Definitions area.

Note: With the processor running at 8 MHz, the RDn line must be asserted for at least 3 clocks to guarantee valid data when reading from the MDAT Machine State Definitions area.

Multiple entries may be used for a given MDAT TypeCode, allowing multiple MDAT Data values to be entered for a given TypeCode.

Data entered for SSSS = 0 will be ignored. Machine State 0 is reserved for definition of behavior when no Machine State match is found or when MDAT qualification is not possible/desired.

Changing MDAT Data will never have any effect on a timer that has already triggered and is counting.

The sequence for tracking MDAT “matches” is as follows:

1. TCLK $07 is received, indicating the previous batch of MDAT’s is complete, and a new batch of MDAT’s is about to arrive.
2. The Match Pointer is updated:
    a. If a match was found in the previous batch of MDAT’s, the Match Pointer is set according to the entry where the first match was found.
    b. If no match was found, the Match Pointer is set to zero.
3. The internal “match” flag is cleared.
4. MDAT is monitored for matches in RAM. The match flag is set if a match is found.
5. TCLK $07 is received, indicating the previous batch of MDAT’s is complete, and a new batch of MDAT’s is about to arrive.
6. etc, etc

0x1800 : 0x18FF – Channel Counter Presets

This address space is broken up as follows:

ADDR[13:0] = 01_1000_NNSS_SSBB, where:

NN = Lower two bits of channel number (0 thru 3 or 4 thru 7)
SSSS = MDAT Machine State Select (0 thru 15)
BB = Byte select (8 bits of a 32-bit value)
- 00 = Byte 0 (Least Significant Byte)
- 01 = Byte 1
- 10 = Byte 2
- 11 = Byte 3 (Most Significant Byte)

Data bytes must be written in groups of four bytes. Data for a 32-bit word is captured with the write to the high byte (BB = 11).

Note: Running at 8 MHz, the processor must wait at least 3 clocks after writing to BB = 11, to guarantee all data is captured by the FPGA, before performing another write operation to the Counter Channel Presets area.

Note: With the processor running at 8 MHz, the RDn line must be asserted for at least 3 clocks to guarantee valid data when reading from the Counter Channel Presets area.

BB = 00 – Byte 0 (LSB)

Bits	Bit Definitions	Value at Reset
7:0	Counter Preset Value, Bits 7:0	Uninitialized

BB = 01 – Byte 1

Bits	Bit Definitions	Value at Reset
7:0	Counter Preset Value, Bits 15:8	Uninitialized

BB = 10 – Byte 2

Bits	Bit Definitions	Value at Reset
7:0	Counter Preset Value, Bits 23:16	Uninitialized

BB = 11 – Byte 3 (MSB)

Bits	Bit Definitions	Value at Reset
7:0	Counter Preset Value, Bits 31:24	Uninitialized

0x2000 – Channel Enable Register

Bits	Bit Definitions	Value at Reset
7:0	Write Bit N to 1 to enable Channel N. Write Bit N to 0 to disable Channel N and cancel any timer in progress.	0x00

0x2800 – Heartbeat Strobe Register

Any access to the Heartbeat Strobe Register will cause the Heartbeat LED to flash once.

Bits	Bit Definitions	Value at Reset
7:0	Unused These bits are unused and will ignored by the FPGA logic.	N/A

0x2801 – Counter Module Reset Register

Any access to the Counter Module Reset Register will cause the Counter Module to reset. All channels will be disabled. Any counters in progress will be cancelled.

Bits	Bit Definitions	Value at Reset
7:0	Unused These bits are unused and will ignored by the FPGA logic.	N/A

0x3000 : 0x3006 – CAMAC Interface

The CAMAC Interface utilizes a 9-bit data bus. This allows the CAMAC Function/Address pair to be captured with a single read. The CAMAC interface address space is broken up as follows:

0x3000 (Read) – Capture CAMAC R[8:1]

Reading address offset 0x00 will capture the Least Significant Byte from the CAMAC R bus (R[8:1]). Reading this address will have no effect on the state of the CAMAC Interface interrupt.

Bits	Bit Definitions
8	Unused
7:0	CAMAC R[8:1]

0x3000 (Write) – Set CAMAC W[8:1]

Writing address offset 0x00 will set the Least Significant Byte of the CAMAC W bus (W[8:1]). Writing this address will have no effect on the state of the CAMAC Interface interrupt.

Bits	Bit Definitions
8	Unused
7:0	CAMAC W[8:1]

0x3001 (Read) – Capture CAMAC R[16:9]

Reading address offset 0x01 will capture the Most Significant Byte from the CAMAC R bus (R[16:9]). Reading this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
8	Unused
7:0	CAMAC R[16:9]

0x3001 (Write) – Set CAMAC W[16:9]

Writing address offset 0x01 will set the Most Significant Byte of the CAMAC W bus (W[16:9]). Writing this address will clear the CAMAC Interface interrupt.

Bits	Bit Definitions
8	Unused
7:0	CAMAC W[16:9]

0x3004 (Read) – Capture Function and Subaddress (F/A)

Reading address offset 0x04 will capture the state of the F and A CAMAC dataway signals. Reading this address will clear the CAMAC Interface interrupt for Functions 9 thru 31. Reading this address will have no effect on the state of the CAMAC Interface interrupt for Functions 0 thru 8.

Bits	Bit Definitions
8	F16
7	F8
6	F4
5	F2
4	F1
3	A8
2	A4
1	A2
0	A1

0x3004 (Write) – Clear Invalid Interrupt

Writing address offset 0x04 will clear the CAMAC interrupt, and no Q will be sent back to the CAMAC controller. Use this to clear an interrupt if an invalid Function or Subaddress is given, or if any other error occurs that does not allow the system to complete the CAMAC command.

Bits	Bit Definitions
8:0	Unused. Data will be ignored.

0x3006 (Write) – Set/Clear Look-At-Me (LAM)

Writing address offset 0x06 set the LAM CAMAC Dataway signal.

Bits	Bit Definitions
8:1	Unused. Data will be ignored.
0	Logic state to set LAM to 1 = TRUE (Low) 0 = FALSE (High)

EEPROM

The C577 module is equipped with an 8k x 8 EEPROM for nonvolatile storage of module settings. The EEPROM is selected with its own chip select, EECSn. All data is written to the EEPROM in the exact same format that it is written to the FPGAs. The memory map for the EEPROM storage is as follows:

Address	Register Definition
0x0000 – 0x07FF	TCLK Trigger Tables, Channels 0 – 3 (FPGA0)
0x0800 – 0x0FFF	TCLK Trigger Tables, Channels 4 – 7 (FPGA1)
0x1000 – 0x10FF	Counter Presets, Channels 0 – 3 (FPGA0)
0x1100 – 0x11FF	Counter Presets, Channels 4 – 7 (FPGA1)
0x1200 – 0x12FF	MDAT Machine State Definitions, Channels 0 – 3 (FPGA0)
0x1300 – 0x13FF	MDAT Machine State Definitions, Channels 4 – 7 (FPGA1)
0x1400	Channel Enables, Channels 0 – 3 (FPGA0)
0x1401	Channel Enables, Channels 4 – 7 (FPGA1)
0x1402	EEPROM Checksum