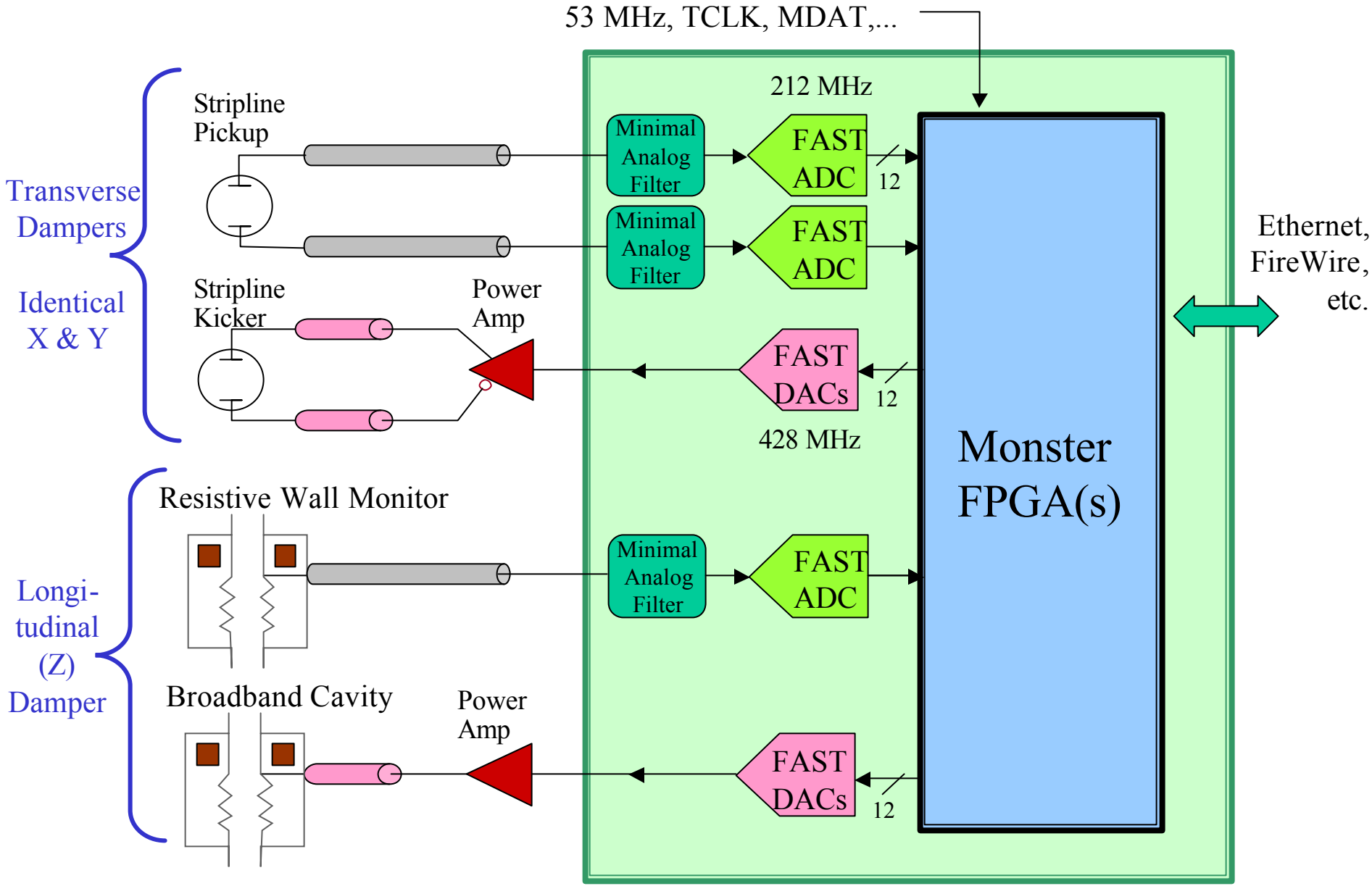
Digital Bunch-by-Bunch Dampers for the Fermilab Main Injector & Recycler

Bill Foster , Dennis Nicklaus,
Warren Schappert, Dave Wildman (FNAL),
Bill Ashmanskas (*ANL / UC*)

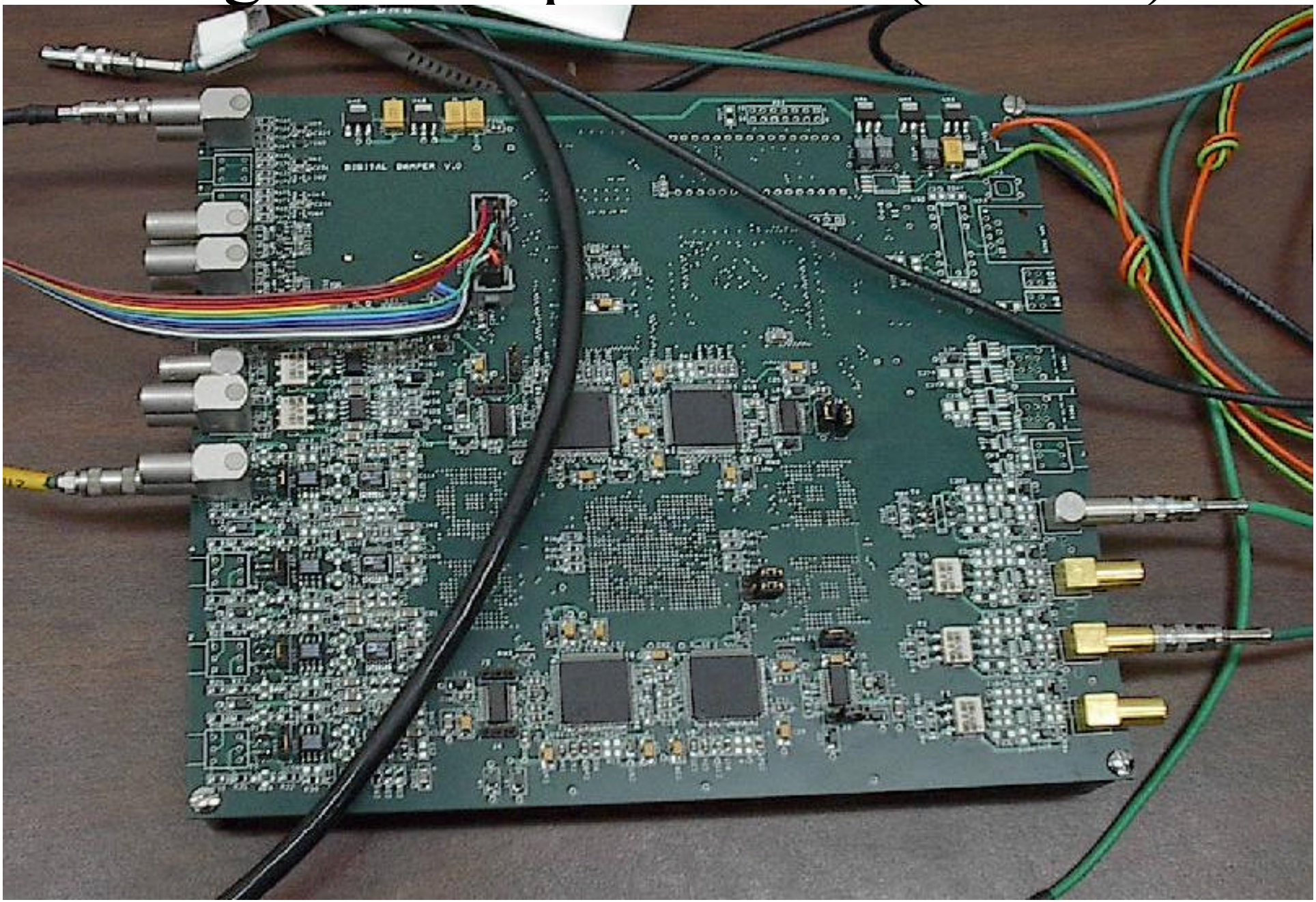
July '03 Lehman Rev.

- Many Beam Types in MI/RR
- 3-coordinate Digital Damper
- Beam Results (transverse)
  - Injection Damping & Emittance Control
  - Resistive-Wall Instability Damping
- Longitudinal Damper Status
  - All parts ready for installation
- Other Applications of this technology

All-Coordinate Digital Damper



Digital Damper Board (~ NIM)



Wide Variety of Beam Dampers Required in MI & Recycler

1) Transverse (X,Y) and Longitudinal

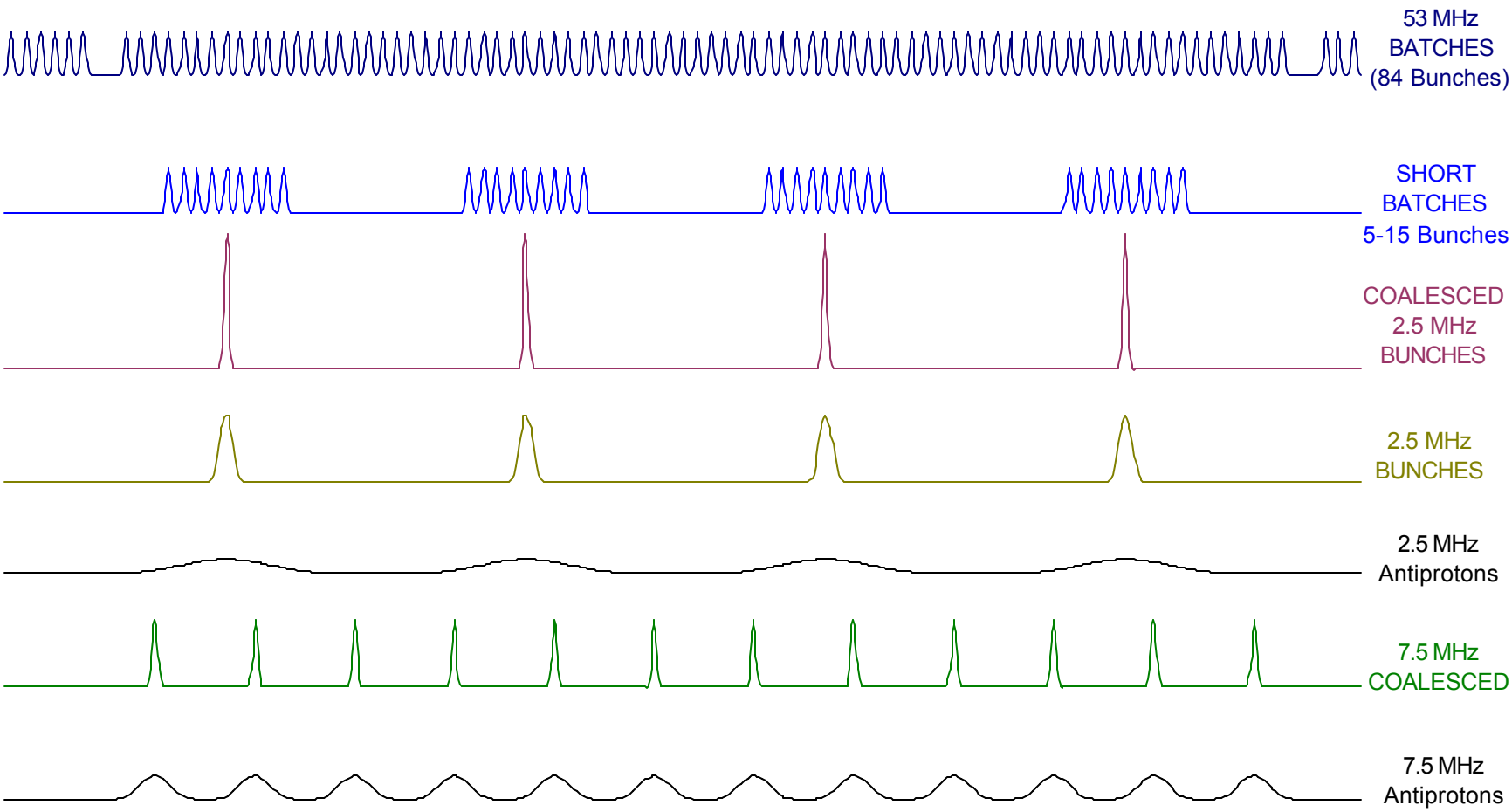
2) 53 MHz, 2.5 MHz, 7.5 MHz, and DC Beam

3) Single Bunches, Full Batches, Short Batches

4) Injection, Ramping, and Stored Beam

5) Pbar and Proton Directions (different timing)

Beam Bunch Structures in Fermilab Main Injector



... plus unbunched DC Beam in Recycler...

Damper Operating Modes

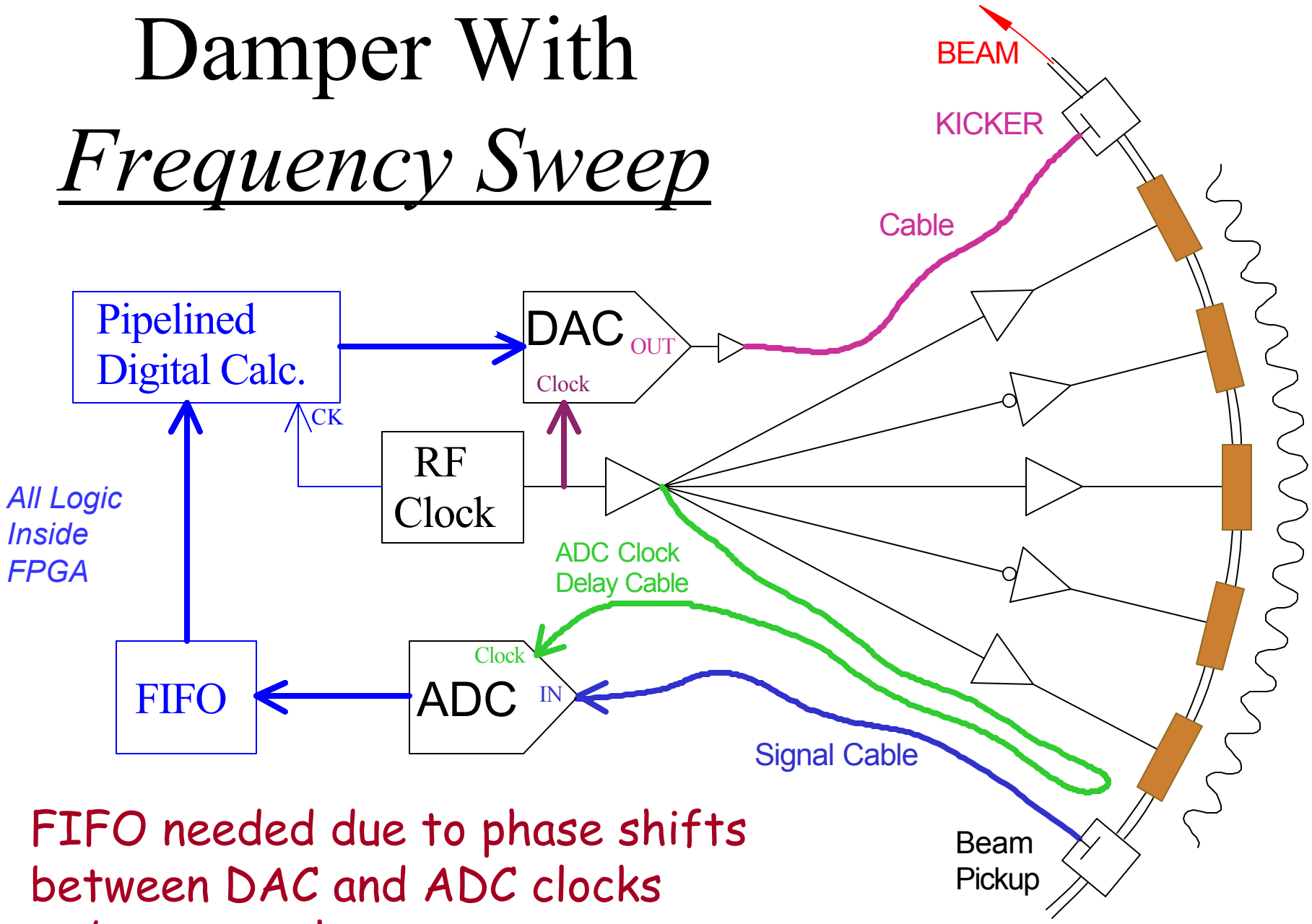
	Booster		Main Inj.		Recycler		Tevatron	
	Pbar	P	Pbar	P	Pbar	P	Pbar	P
53 MHz Full Batches		X		X		C		
53 MHz Short Batches			X	X				C
53 MHz Coalesced Bunch			X	X			X	X
2.5 MHz Batch (4)			X	C	X	C		
7.5 MHz Batch (12)			X	C				
DC Beam					X	C		

X = Operation **C** = Commissioning & Tuneup

Advantages of Digital Processing

- Digital filters more reproducible (=>spares!)
- Inputs and Outputs clearly defined (& stored!)
  - filters can be developed & debugged offline
- Digital filter can also operate at multiple lower frequencies …only ADC & DAC are shared.
- Command, Control, Clock & Communications Logic is fully integrated into Digital Processing

Damper With *Frequency Sweep*



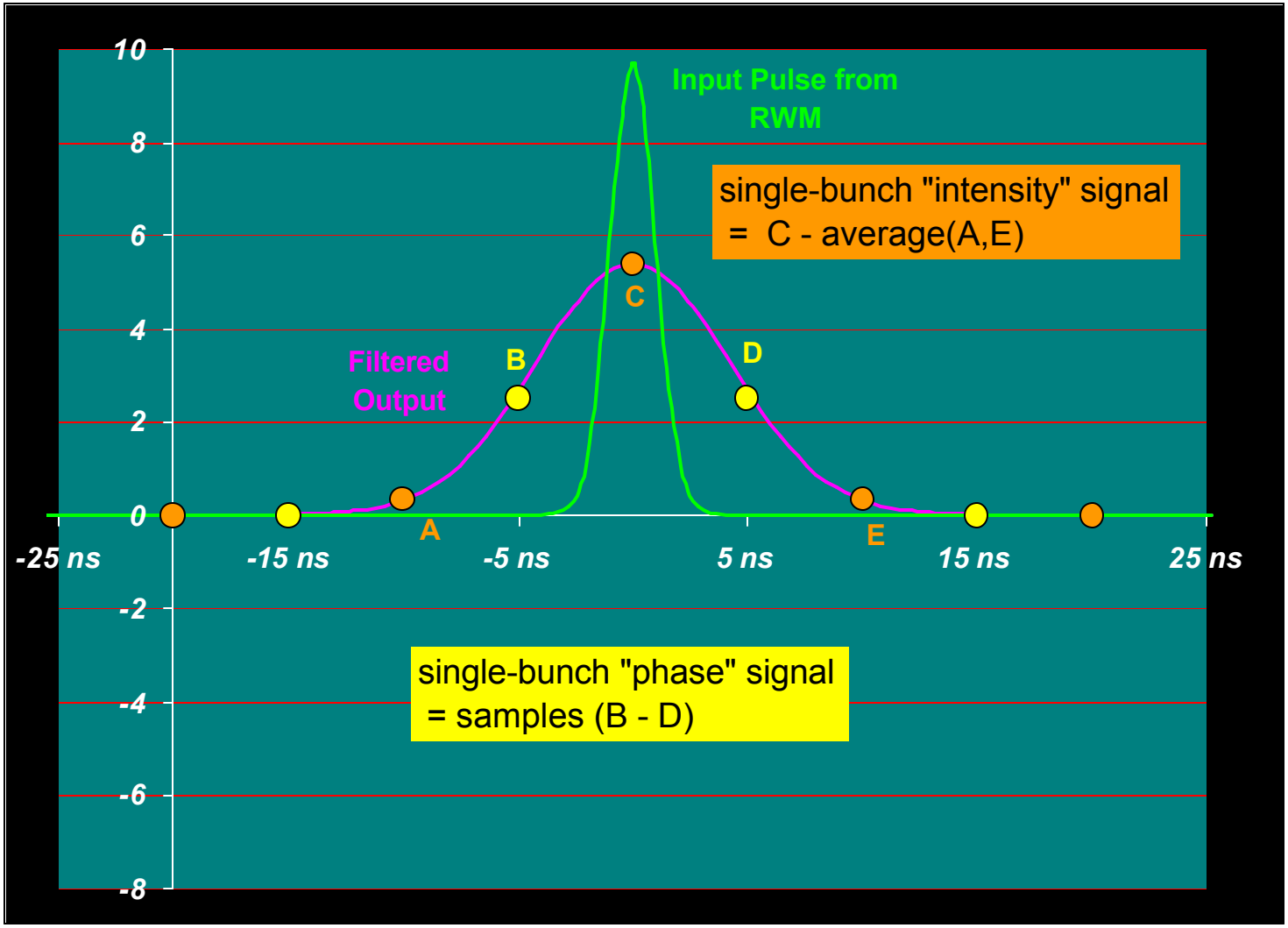
FIFO needed due to phase shifts between DAC and ADC clocks as beam accelerates

Q: What ADC Clock Speed is needed?

A: 4x RF Bunch Frequency

- Minimum needed for bunch-by-bunch Phase and Amplitude measurement
- In frequency domain, 4x RF sampling measures both *in-phase* and *quadrature* components.
- For Fermilab's 53 MHz RF ✍ 212 MHz ADC's

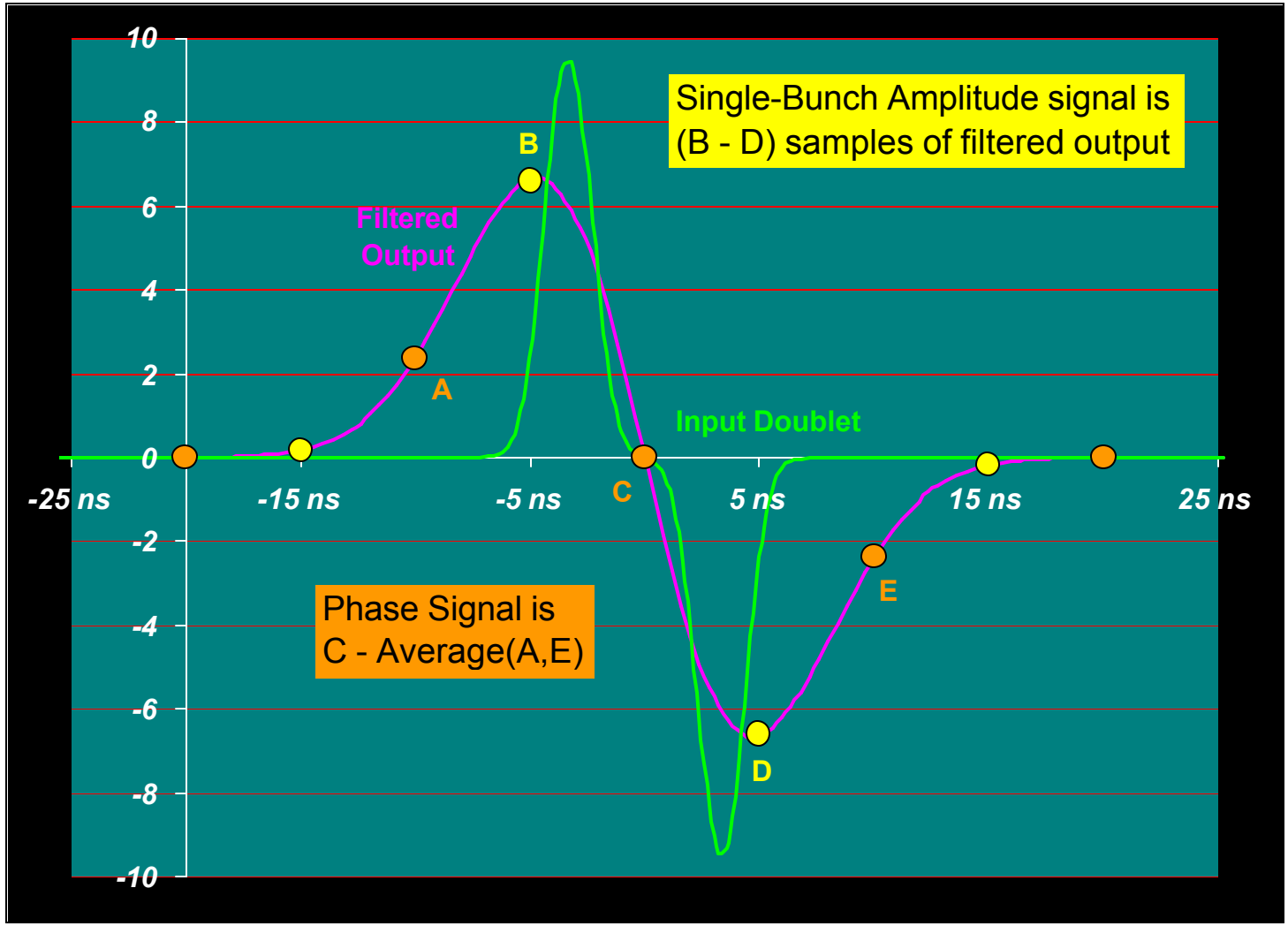
212 MHz Sampling of RWM Pulse



Low-pass Filter Spreads signal +/-5ns in time so it will not be missed by ADC

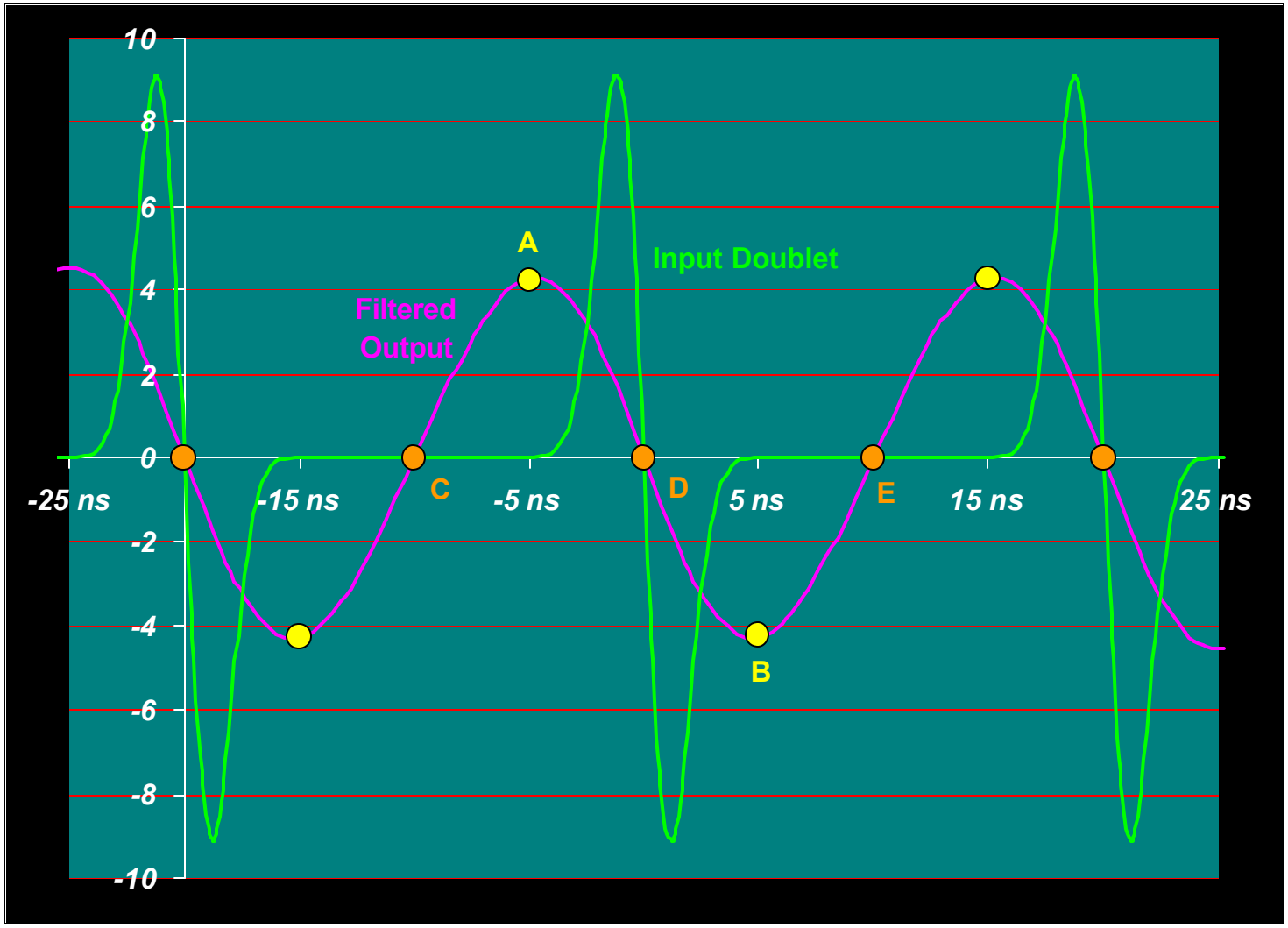
Filter Reduces ADC Dynamic Range requirement, since spike does not have to be digitized

212 MHz Sampling of Stripline Signal



Roles of "Phase" and "Amplitude" signals are reversed from unipolar case.

Repetitive Waveform looks like simple sine wave, but contains bunch-by-bunch phase and amplitude



"A - B" gives bunch-by-bunch "in-phase" signal

"D - (C+E)/2" gives bunch-by-bunch "out-of-phase" or "quadrature" signal

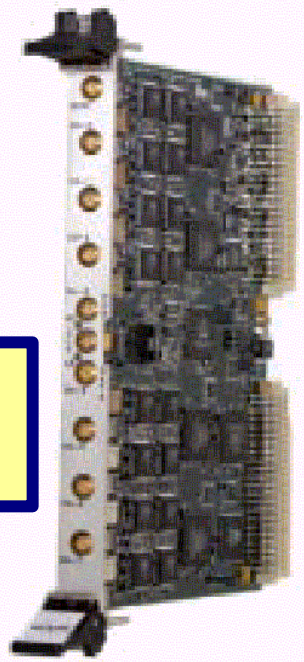
Vector Sum sqrt(I**2 +Q**2) is insensitive to clock jitter

Echotek Card Used for Initial Dampers

ECHOTEK CORP.

EIGHT CHANNEL
ANALOG TO DIGITAL CONVERTER
~~WITH DIGITAL RECEIVER~~

ECDR-814/X-AD



✍ 212 MHz DAC Daughter Card (S. Hansen/ PPD)

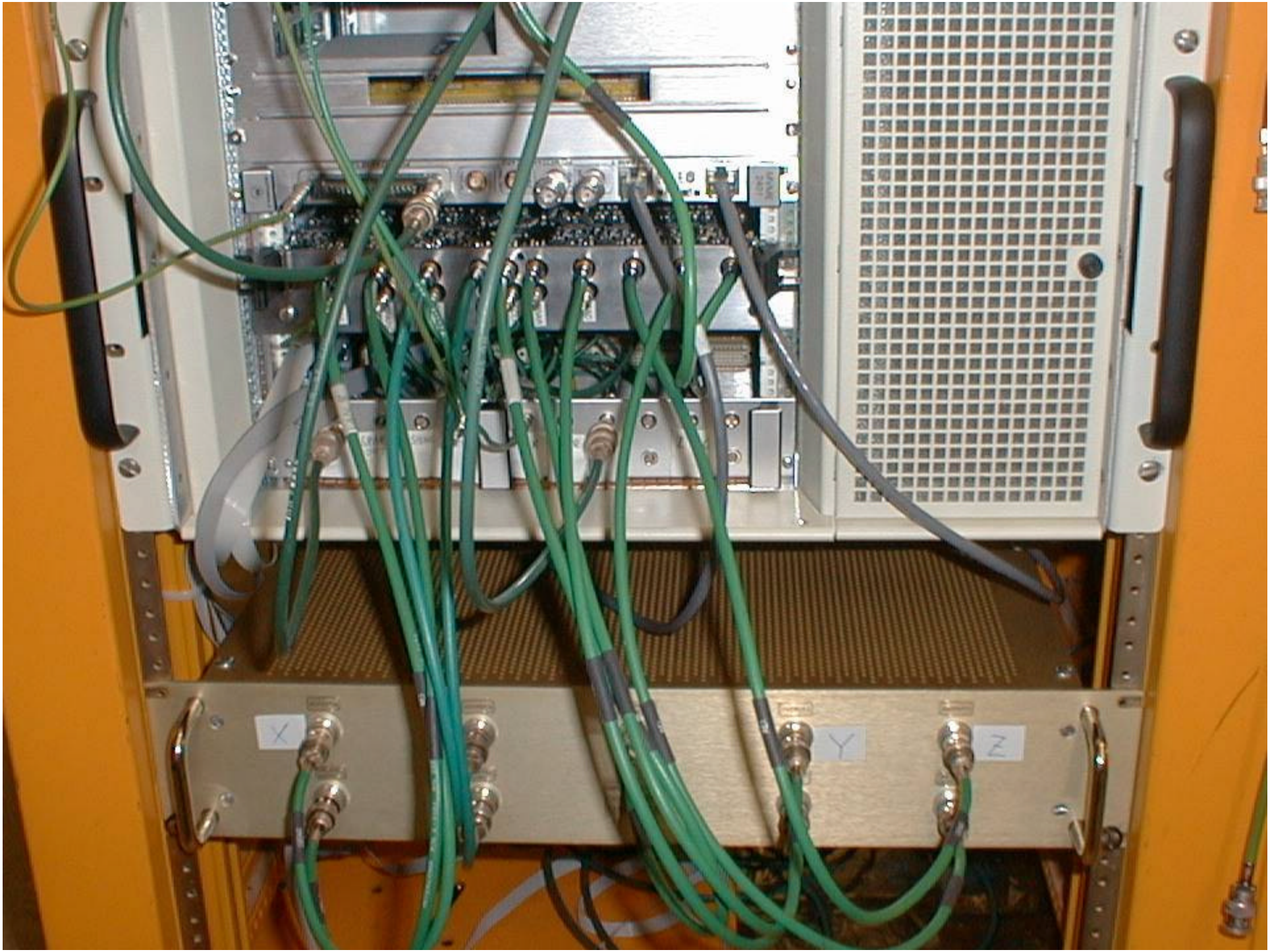
FEATURES

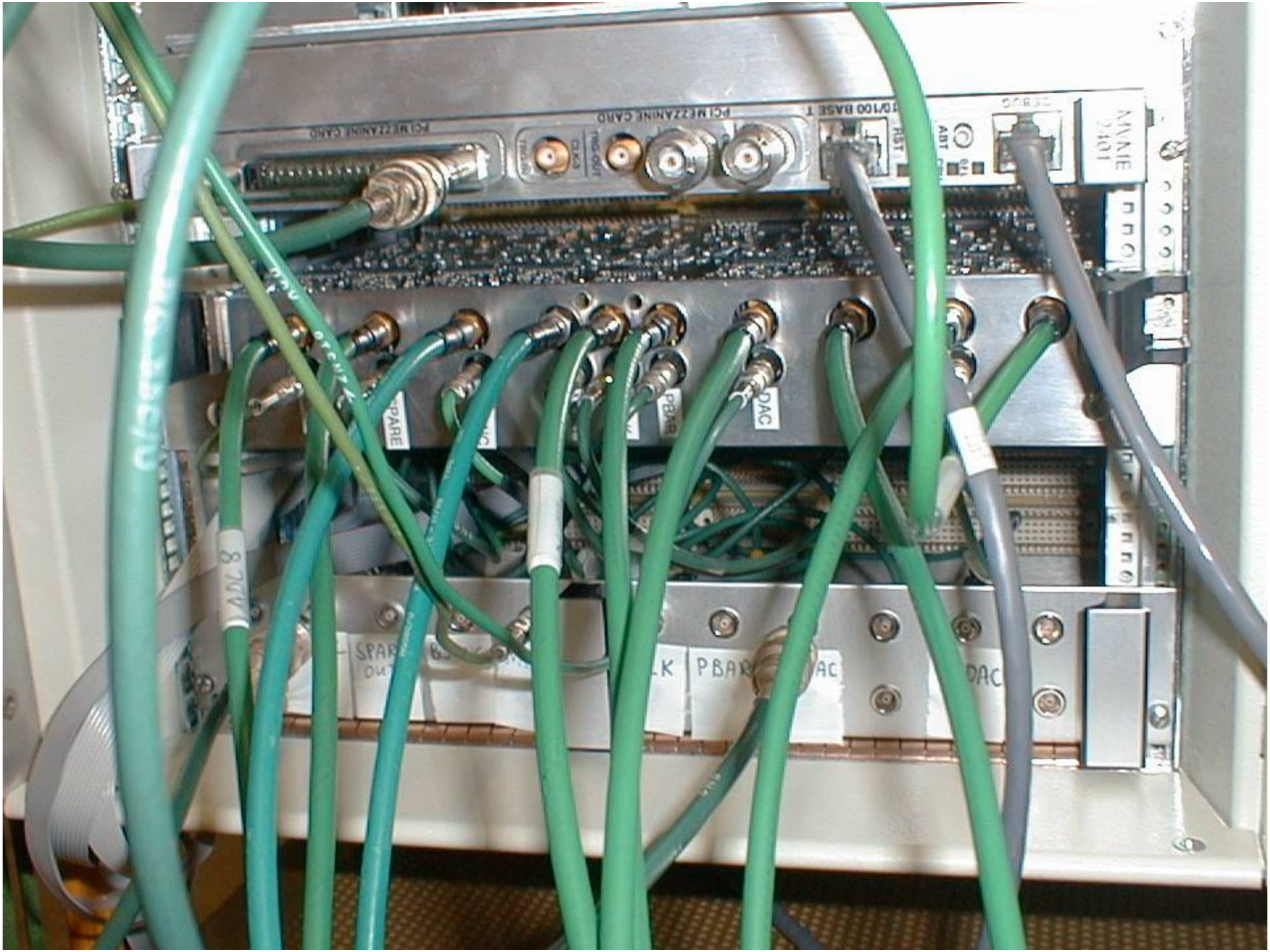
* 8 IF INPUTS
* SIMULTANEOUS SAMPLING
* EIGHT ANALOG TO DIGITAL CONVERTERS (ANALOG DEVICES AD6644, 14 BIT, 65 MSPS) *105 MSPS* *AD6645*
* SFDR > 90 dB FS
* HEADER INSERTION
* VME 64X, SINGLE SLOT
* RACE++ OUTPUT
* AVAILABLE AS A/D CONVERTER AS AN 8, 4, OR 2 CHANNEL MODULE
* VARIABLE GAIN (~ -10 TO +20 dB) OR LOW PASS FILTER

- Echotek Board Originally Built to SLAC Design Specification
- 65MHz DDC version to be used for RR BPM upgrade
- 105 MHz version (with DAC "daughter card") used for Dampers

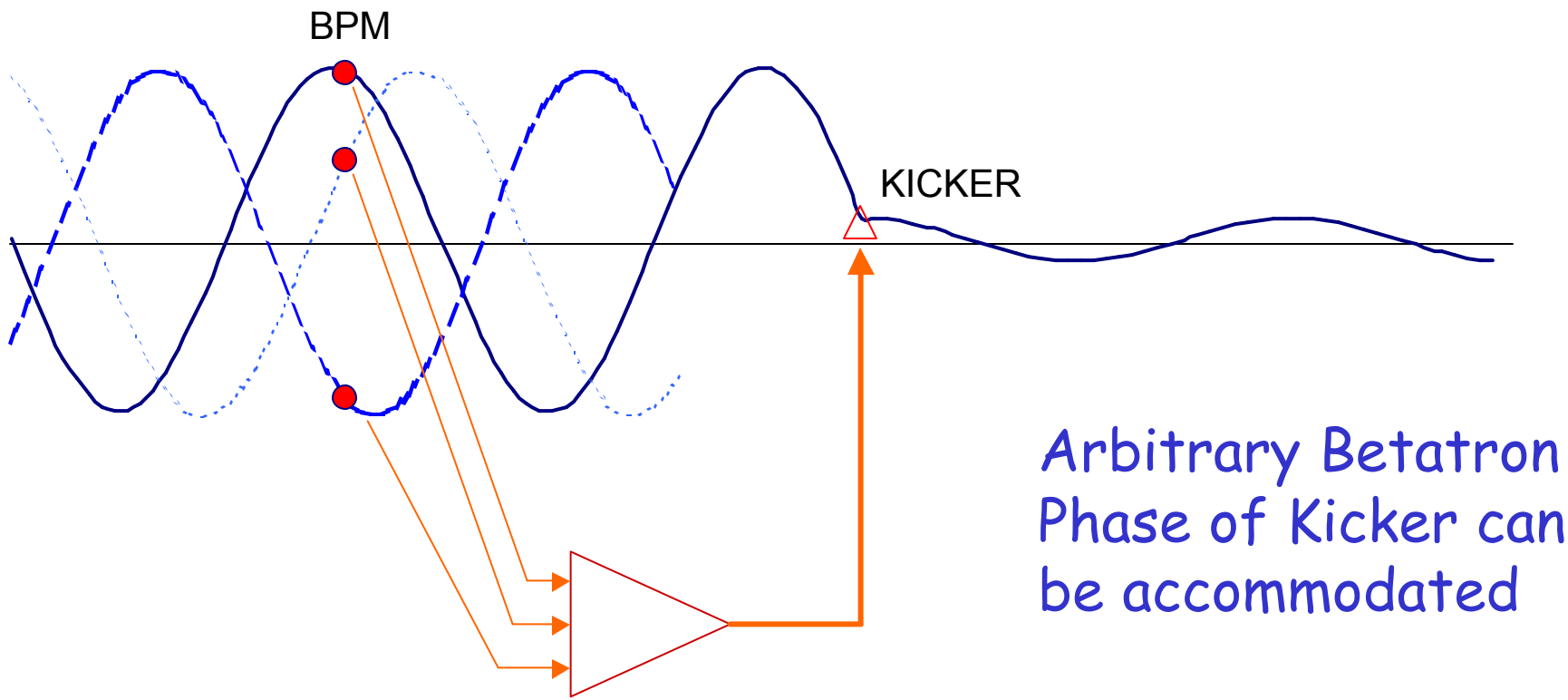
Butchering the Echotek Board

- Scorched-Earth FPGA rewrite (GWF)
  - ~65 pages of firmware since Jan '03
- 212 MHz DAC "Daughtercard"
  - Sten Hansen & T. Wesson (PPD)
  - 3 channels for X,Y,Z
- 212 MHz Output FIR (W. Schappert, RFI)
  - Pre-emphasis compensation for analog outputs
  - Prototype for 424 MHz output on final board
- Input Buffer Amp/Splitter Box (Brian Fellenz,RFI)


X
Y
Z

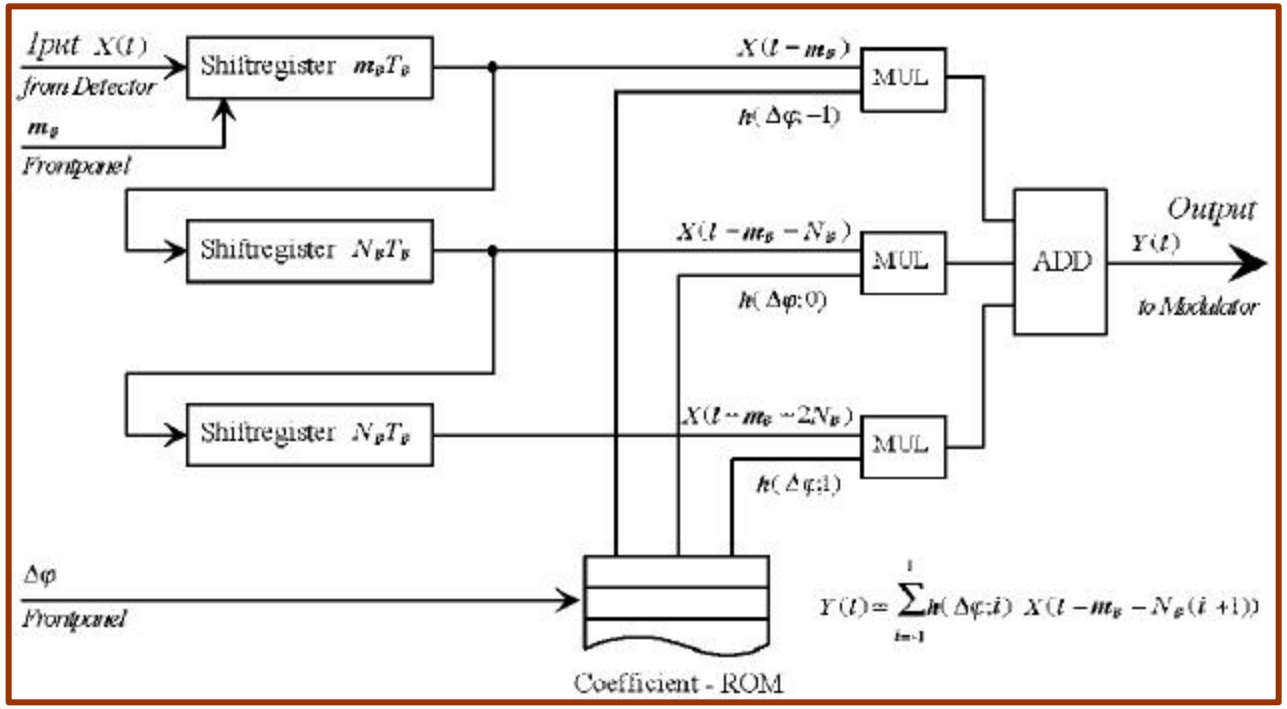

PCI MEZZANINE CARD
PCI MEZZANINE CARD
10/100 BASE T
MVME
2401
SPARE
PBAR
DAC
PBAR
DAC
DAC

3 - Turn Filter for Transverse Damper



- Damper kick is calculated from single BPM position reading on 3 successive turns.

HERA-P Damper uses a 3-turn Digital FIR Filter



Klute, Kohaupt et. al. EPAC '96

- Digital Bunch by Bunch @ 96ns Spacing

"Universal-Damper" Application: Signal Processing Steps (transverse)

Echotek Board

1) Bandwidth-Limit input signal to ~53 MHz
2) 14 Bit Digitization at 106 MHz or 212 MHz

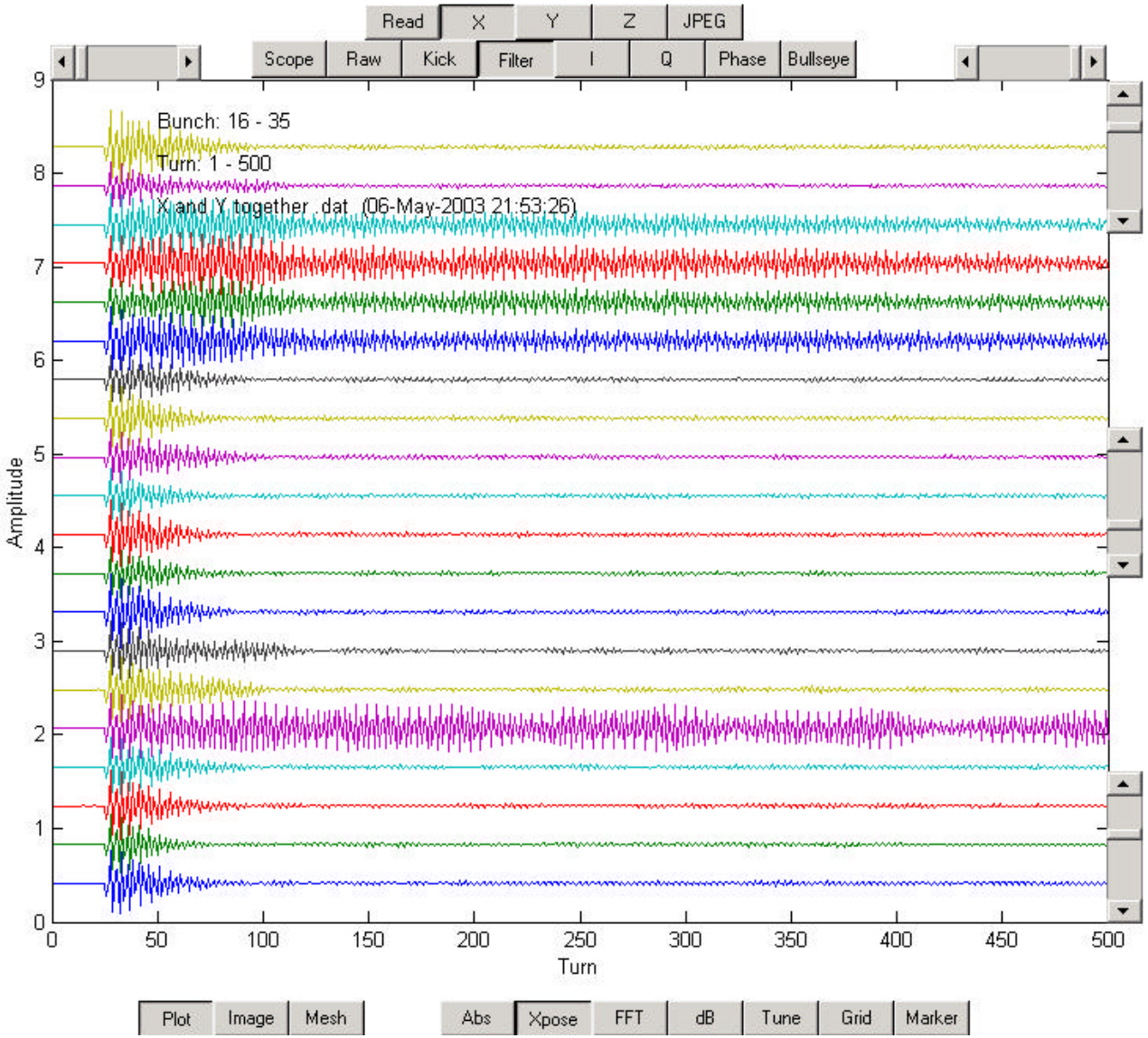
Inside FPGA

3) FIR filter to get single-bunch signal
4) Sum & Difference of plate signals
5) Multi turn difference filter (FIR) w/delay
6) Pickup Mixing for correct Betatron Phase
7) Bunch-by-bunch gain, dead band etc.
8) Timing Corrections for Frequency Sweep
9) Pre-Distortion for Kicker Power Amp

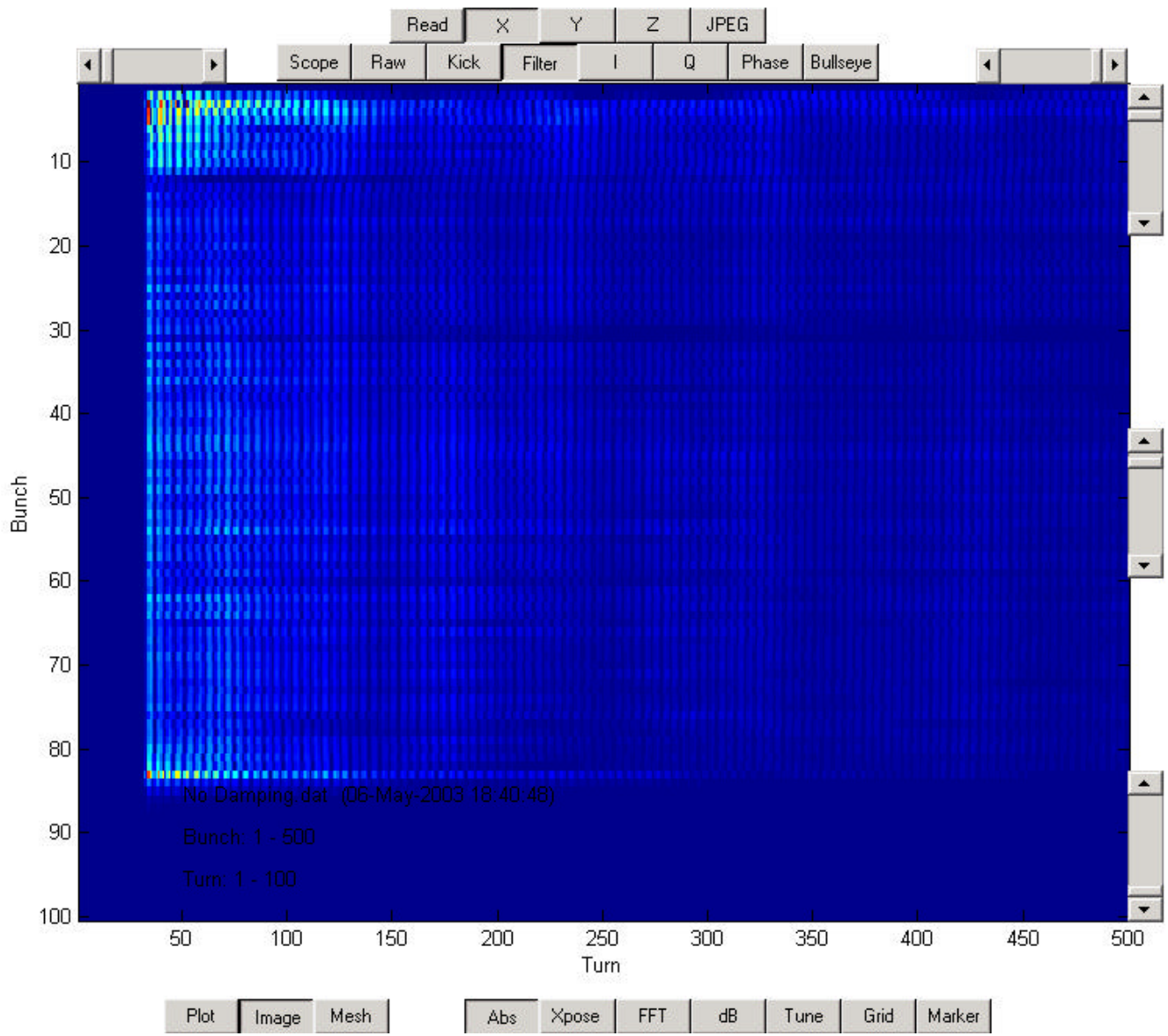
Buy

10) Power Amp for Kicker

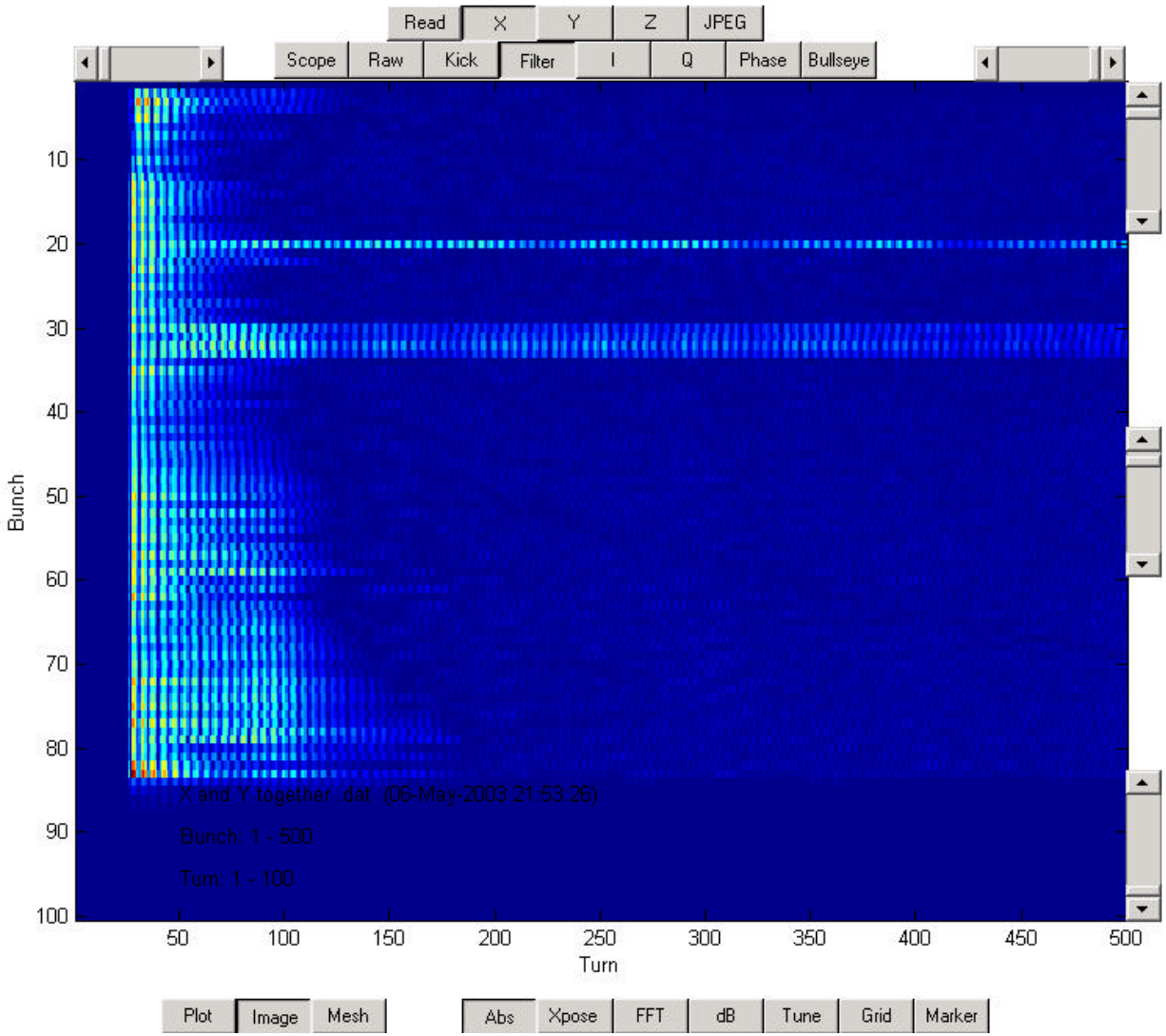
Undamped, Damped, and Anti-Damped Bunches



No Damping

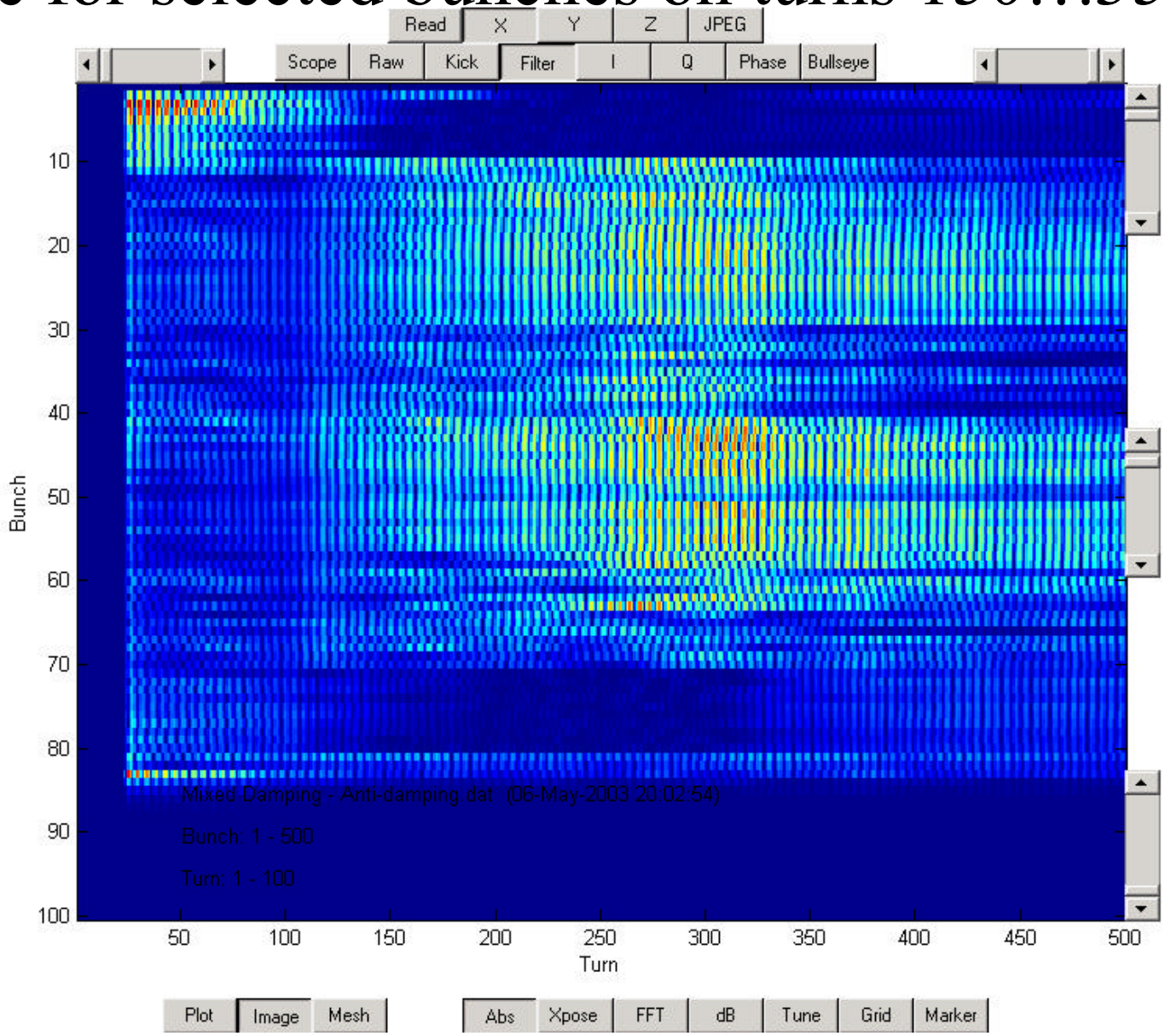

Read
X
Y
Z
JPEG
Scope
Raw
Kick
Filter
I
Q
Phase
Bullseye
Bunch
10
20
30
40
50
60
70
80
90
100
No Damping.dat (06-May-2003 18:40:48)
Bunch: 1 - 500
Turn: 1 - 100
50
100
150
200
250
300
350
400
450
500
Turn
Plot
Image
Mesh
Abs
Xpose
FFT
dB
Tune
Grid
Marker

Undamped, Damped, and Anti-Damped Bunches



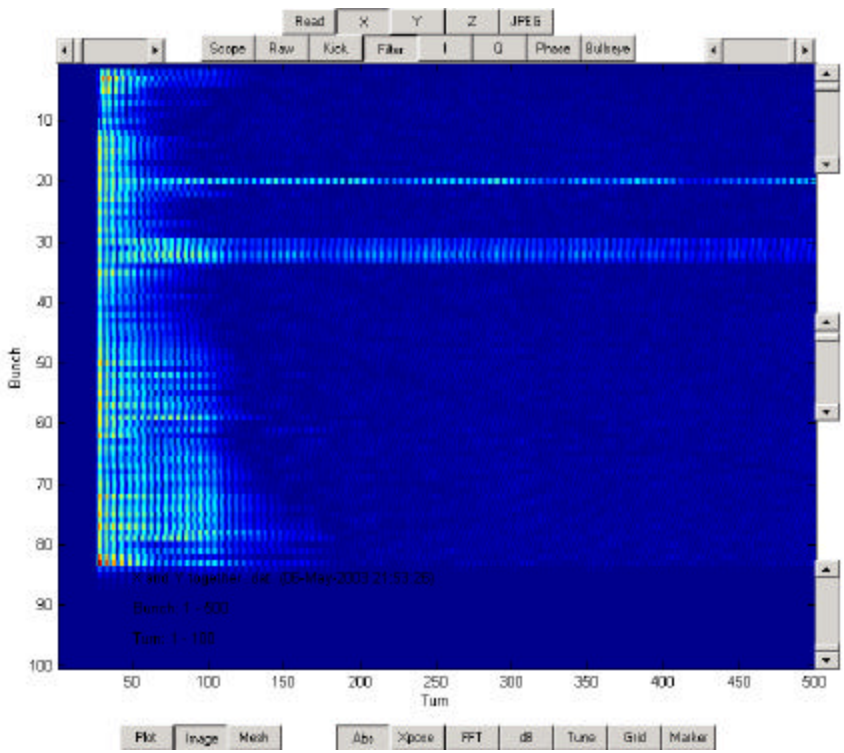
Anti-Damping

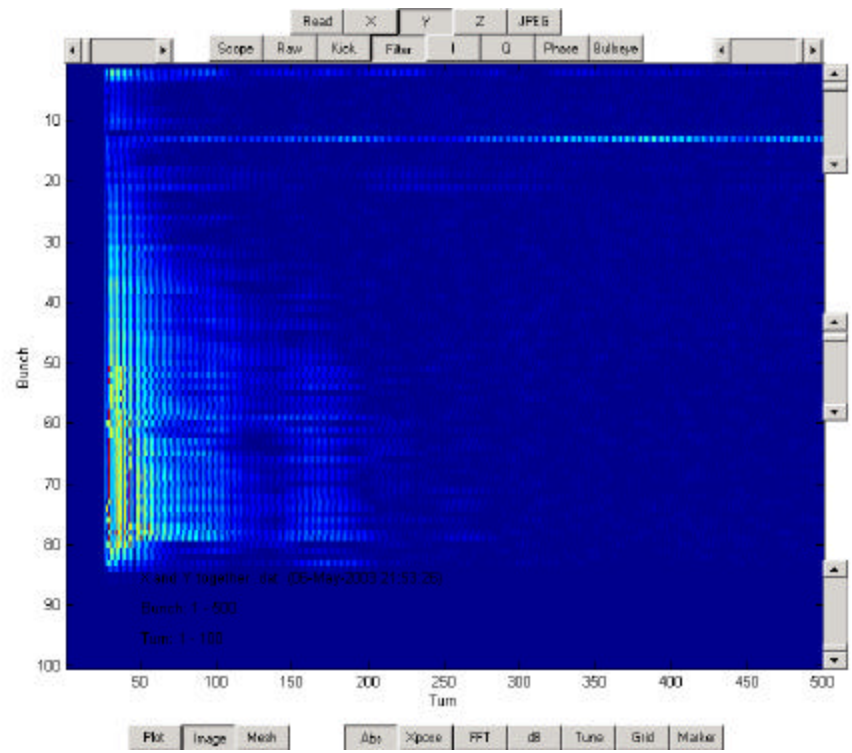
(active for selected bunches on turns 150…350)



Simultaneous X and Y Damping

...essentially no crosstalk





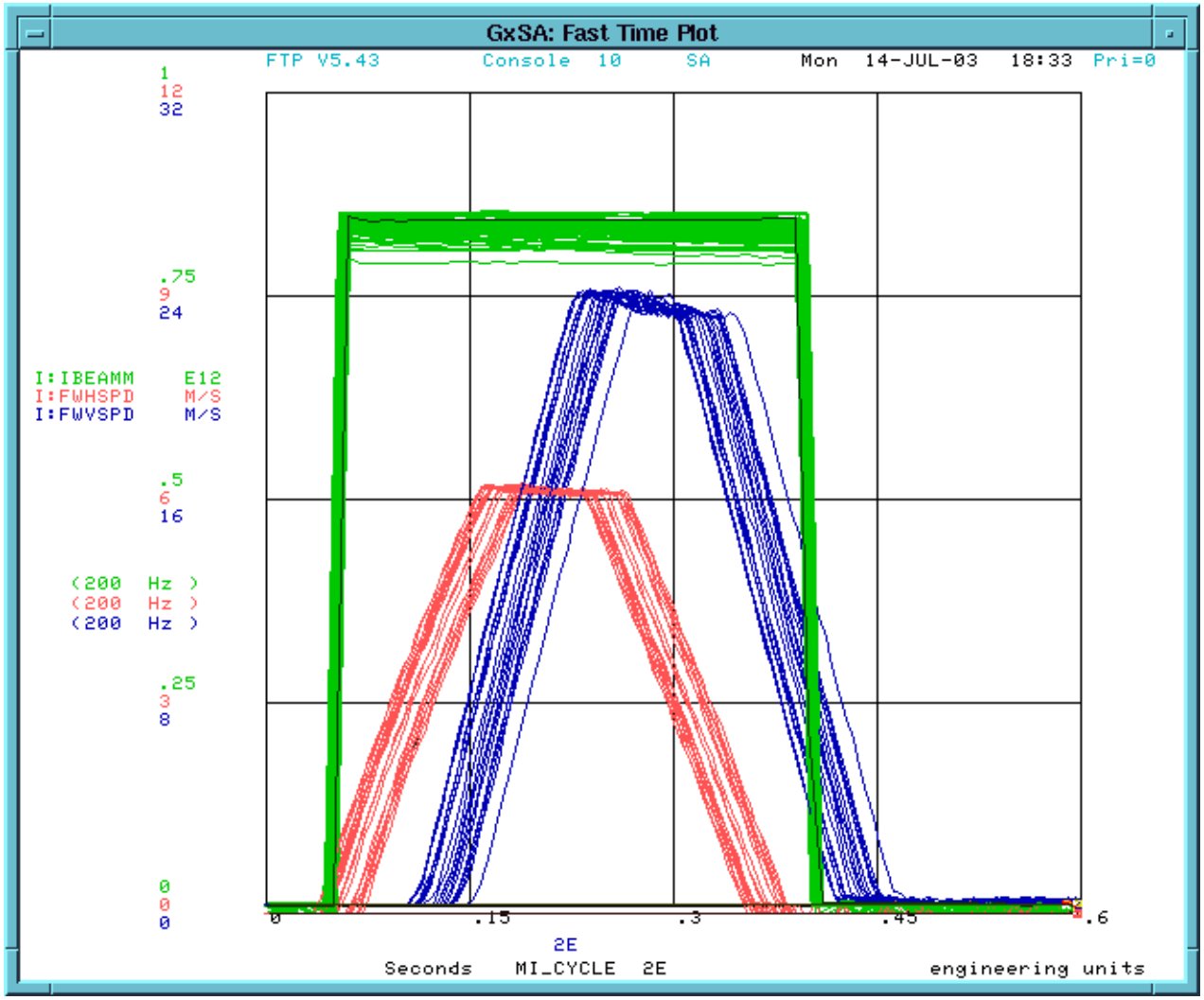
Damper Control of Transverse Emittances
(reason for injection damper)

1. Measure nominal transverse emittances at 8 GeV injection (with flying wires).
2. Screw up injection to blow emittances.

   (Mis-tune injection Lambertson: ~3 mm inj. osc.)
3. Turn on Dampers to recover emittances.

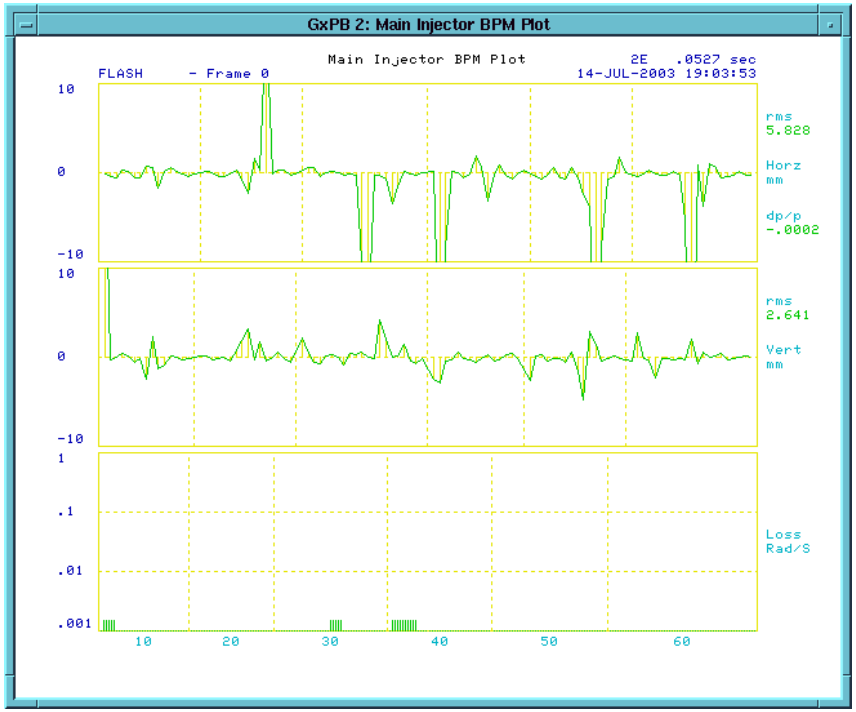
Logbook: ***http://www-bd.fnal.gov/cgi-mach/machlog.pl?nb=mi02&action=view&page=544&scroll=false&load=no***

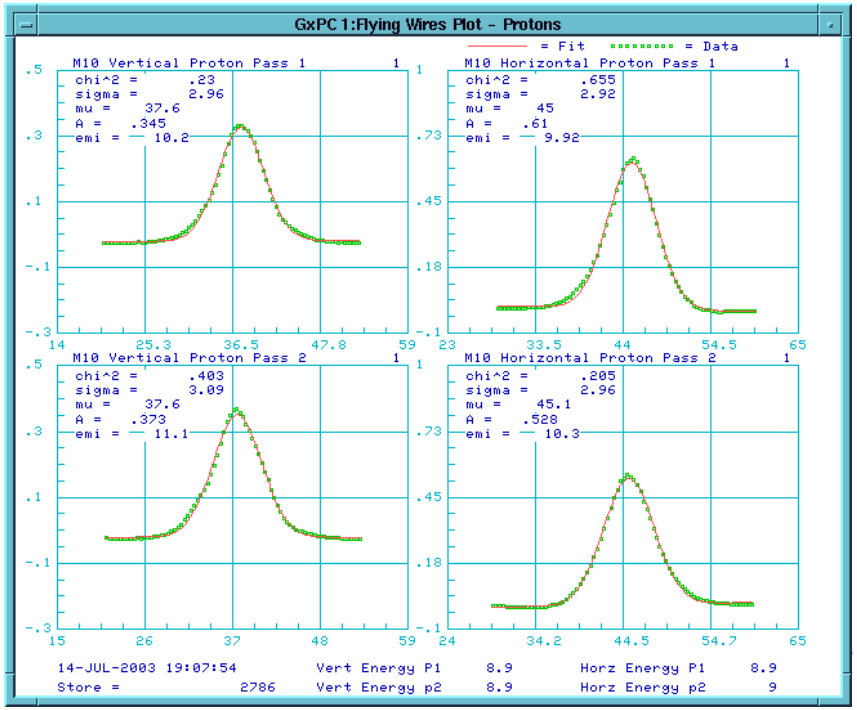
8 GeV Emittances Measured with Flying Wires



- Fly wires ~0.2 sec. after injection

(filamentation complete)





1) Nominal Injection

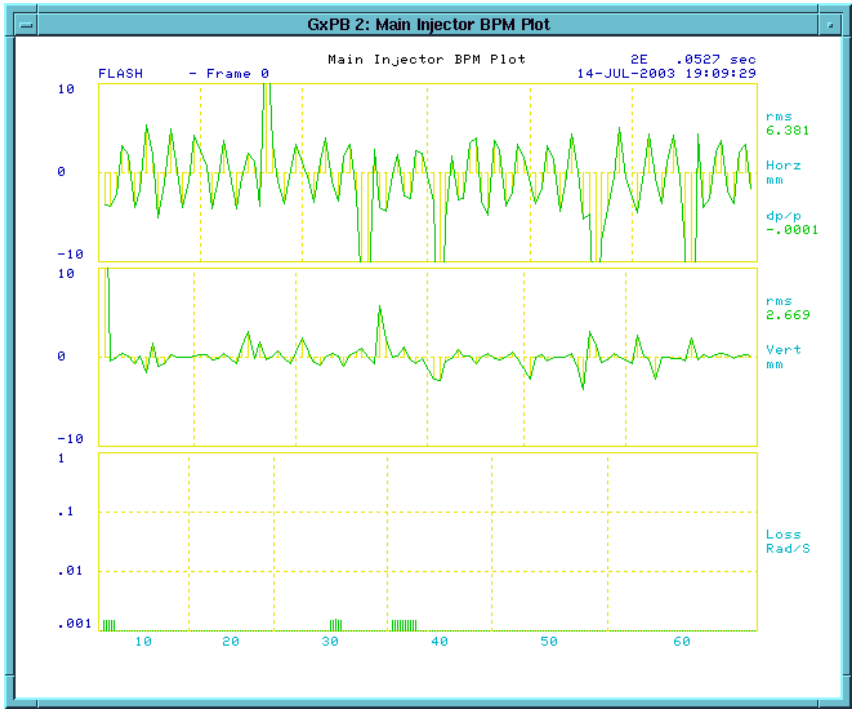
- Orbit Oscillations < 0.5mm
- Emittances:

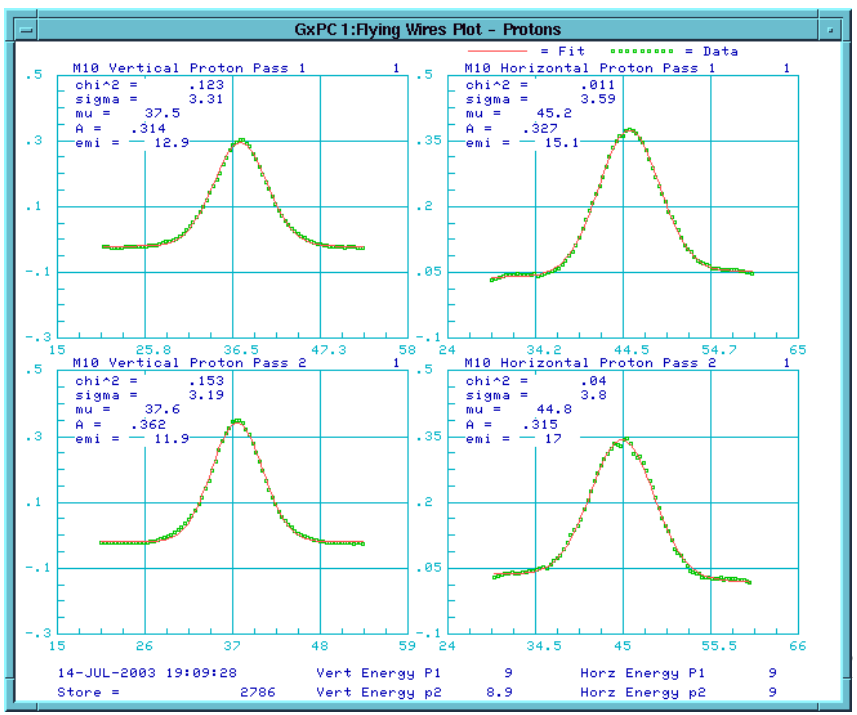
$e_X \sim 10.9$ pi

$e_Y \sim 10.8$ pi

(95% norm)

Dampers - G. W. Foster



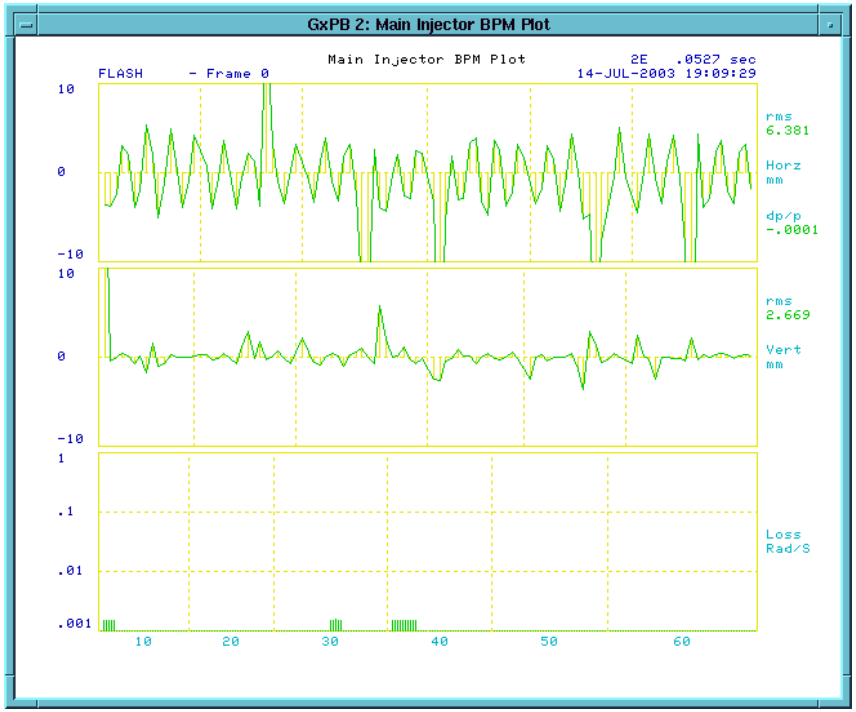


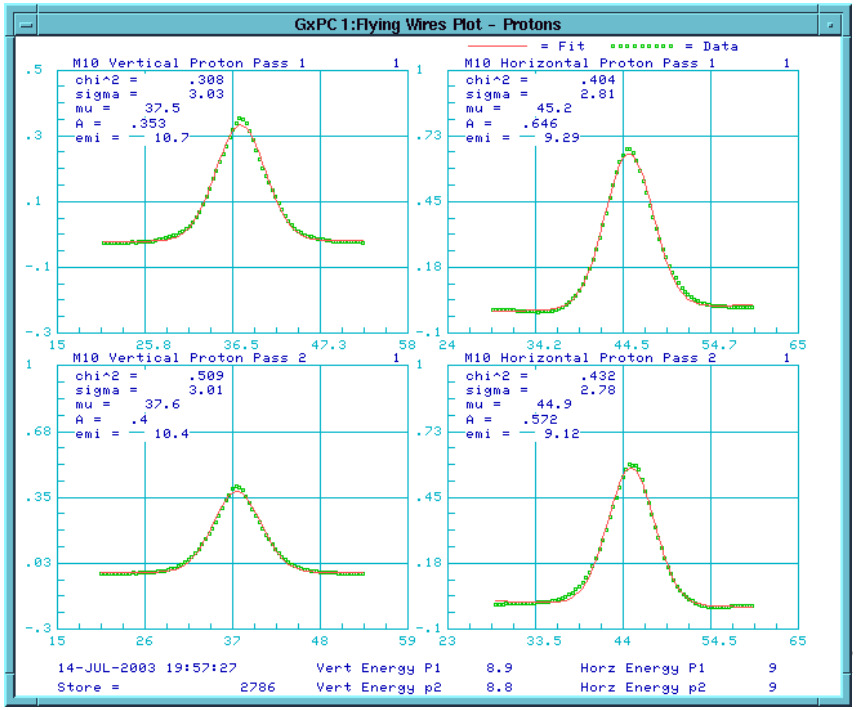
2) Mis-Steered Injection Lambertson

- Orbit Oscillations
  3 ~ 4 mm (X)

- Emittances:
  $e_X \sim 16$ pi
  $e_Y \sim 12$ pi
  (95% norm)

Dampers - G. W. Foster





Dampers ON

- Injection Oscillations still 3~4 mm
- ***Damped by bunch-by-bunch damper***
- ***Emittances Return to Normal:***

$e_X \sim 9.0$ pi

$e_Y \sim 10.1$ pi

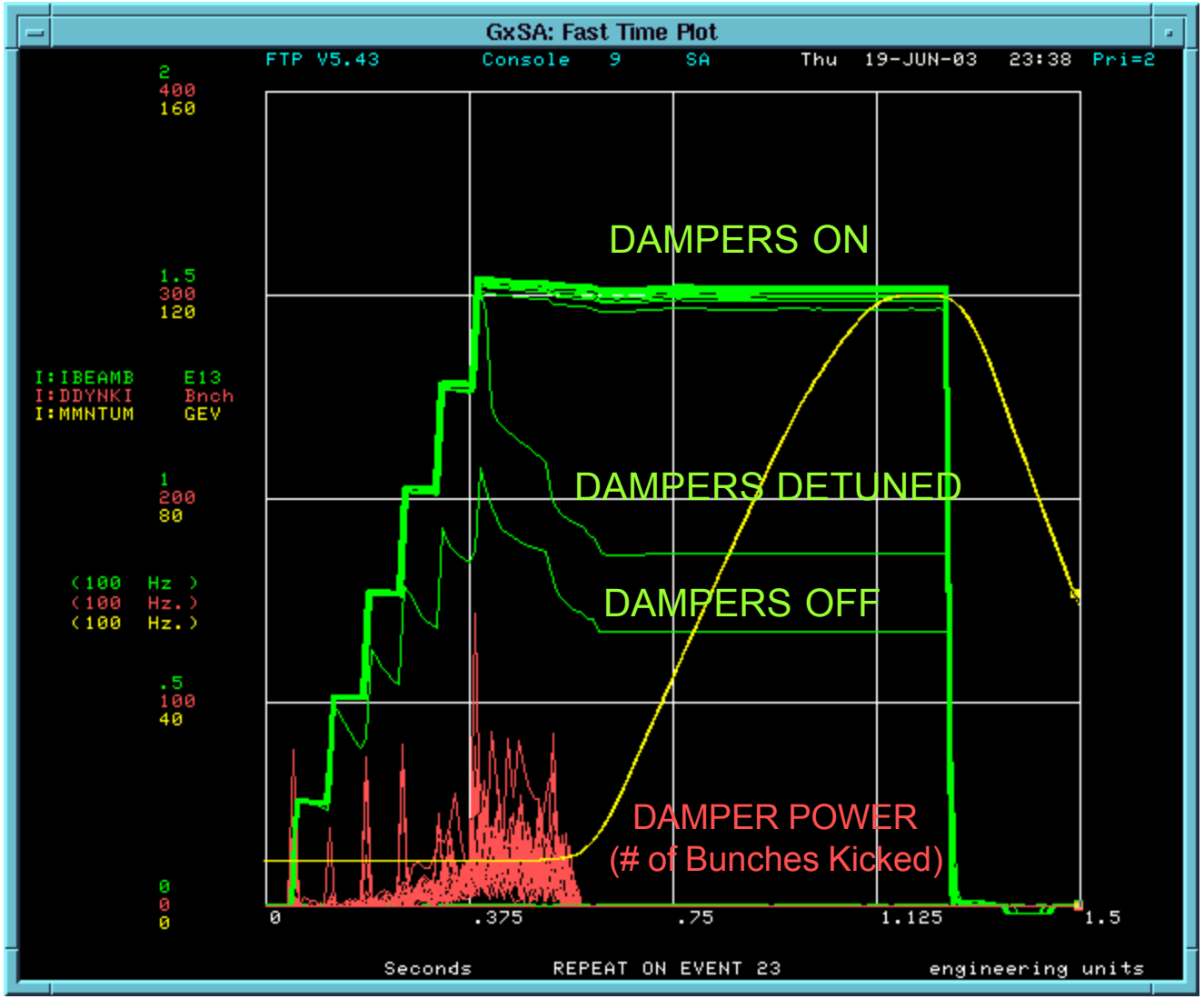
(95% norm)

Damper Control of Multi-Bunch Instabilities

(Resistive-Wall Transverse Instability Damper)

1. Historically limiting factor in Proton intensities (…important for NUMI)
2. Can be partially controlled via chromaticity
3. Bunch-by-bunch beam dampers are also effective on all CB transverse modes

Transverse Instability Damping: Bunch-by-Bunch Damping of Multiple-Batches (NUMI)



- 6 Batches
- Intensity for first tests limited to ~1.5E13 by RF Trips
- Lowered H,V chromaticity to (-8,-8) to incite instability/losses
- Dampers worked immediately to remove losses

Bunch-By-Bunch Control RAM (in FPGA Firmware)

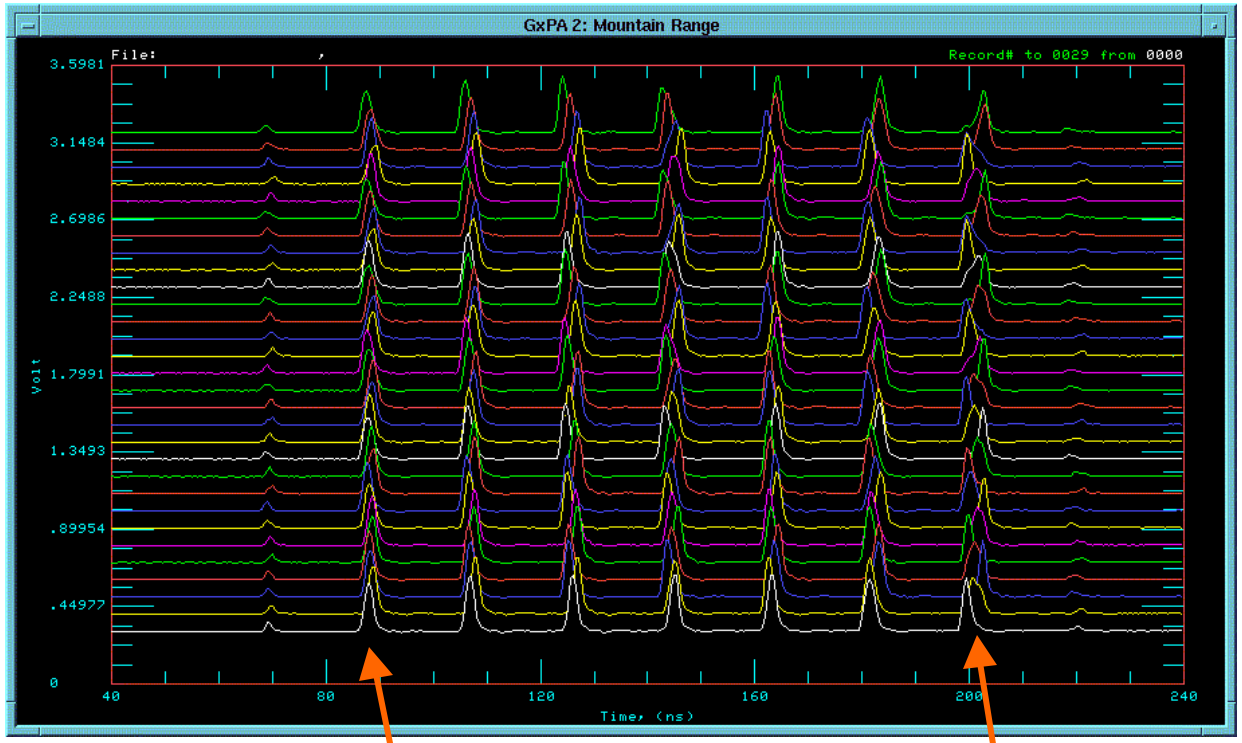
- Bunch-by-bunch Damping Gain
- Damping or Anti-Damping
- Pinger with Programmable Tune, Timing…
- Digital Random Noise Injected Into any Bunch

Blowing Selected Bunches out of the Machine (in X,Y, or both)

Longitudinal Damper in Main Injector

1. Benefits to Bunch Coalescing for Collider
   - "Dancing Bunches" degrade Proton coalescing and $e_{Long.}$
   - Affects Lum directly (hourglass) and indirectly (lifetime)
2. Benefits for Pbar Stacking Cycles
   - Bunch Rotation is generally turned off ! (x1.5 stack rate?)
   - Slip stacking will be difficult with current CB from Booster
3. Needed for eventual NUMI operation

Longitudinal Beam Instability in MI



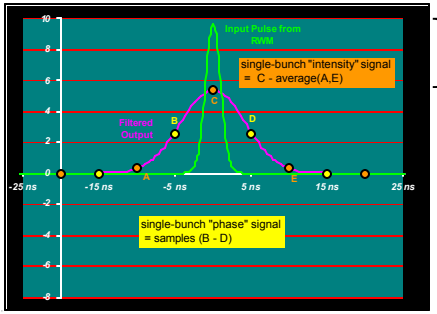
D. Capista,
D. Wildman

First Bunch ~ OK

7th Bunch Trashed

- Occurs with as few as 7 bunches (out of 588)
- Prevents low emittance bunch coalescing and efficient Pbar bunch rotation

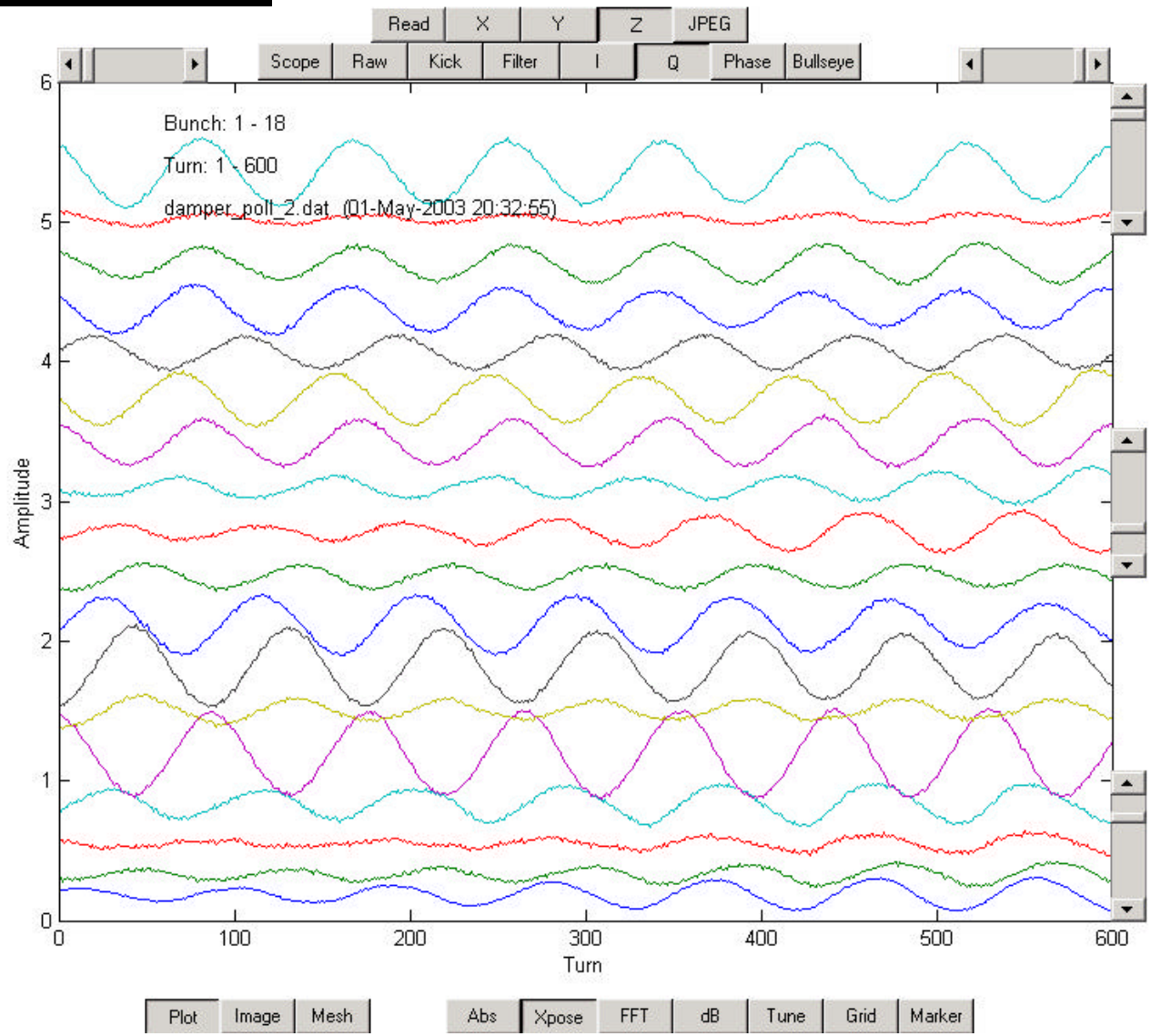
- Driven by cavity wake fields within bunch train
- Seeded by Booster & amplified near MI flat top.



Measured Bunch-By-Bunch Phase

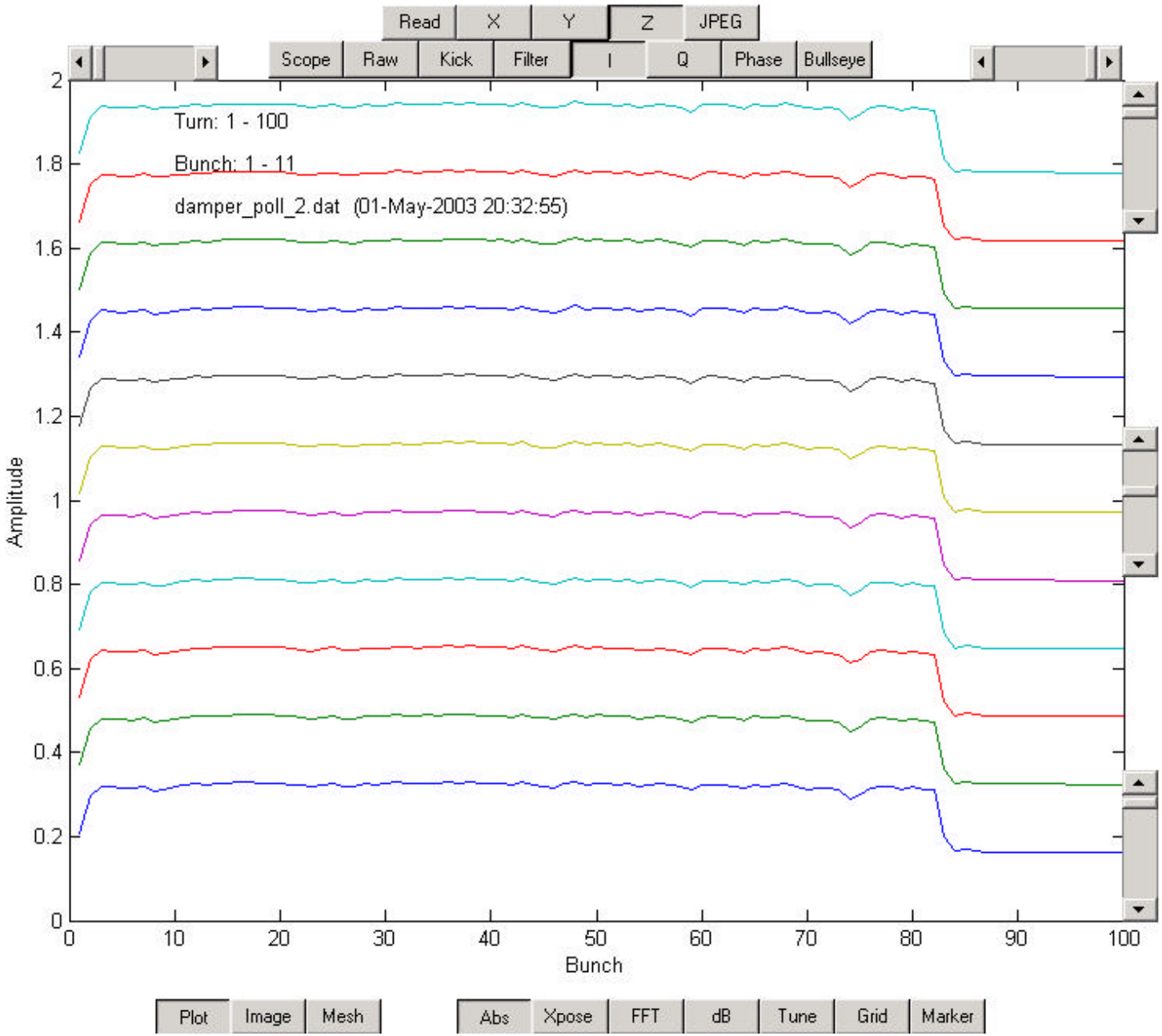
(Longitudinal Quadrature Signal)

vs. Turn Number



- Digital Damper Provides good bunch-by-bunch phase measurement
- Damping kick calculated cleanly and correctly

Bunch-by-Bunch Intensity vs. Bunch Number



Longitudinal Damper Broadband RF Cavities
3 New Cavities, Similar to Recycler,
With Superior HF Response - (*Wildman)*

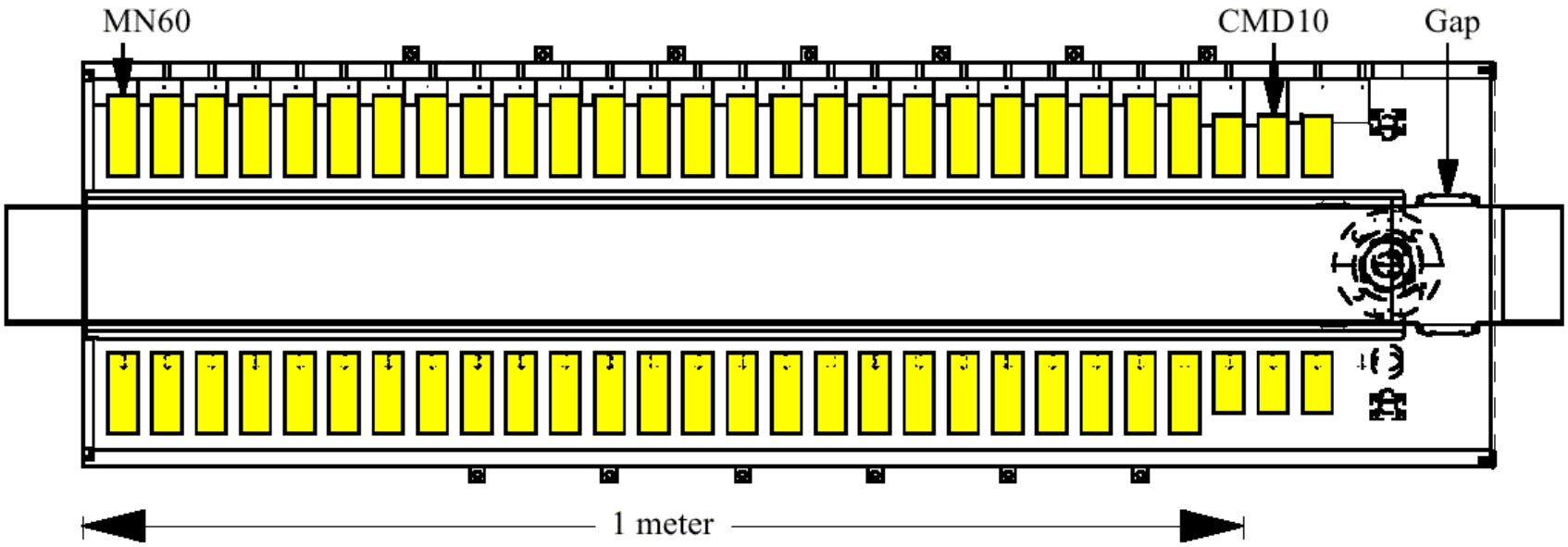


Figure 1: Schematic drawing of Recycler Wideband RF Cavity

Non-Resonant Cavity looks like 50-Ohm Load in parallel with a large Inductor

MAIN

Foster's Rules of Project Management

#1 - Order the Cables.

#2 – Order the Ferrite.

Everything else will take care of itself.

FRAGILE

AR Wideband Power Amplifiers

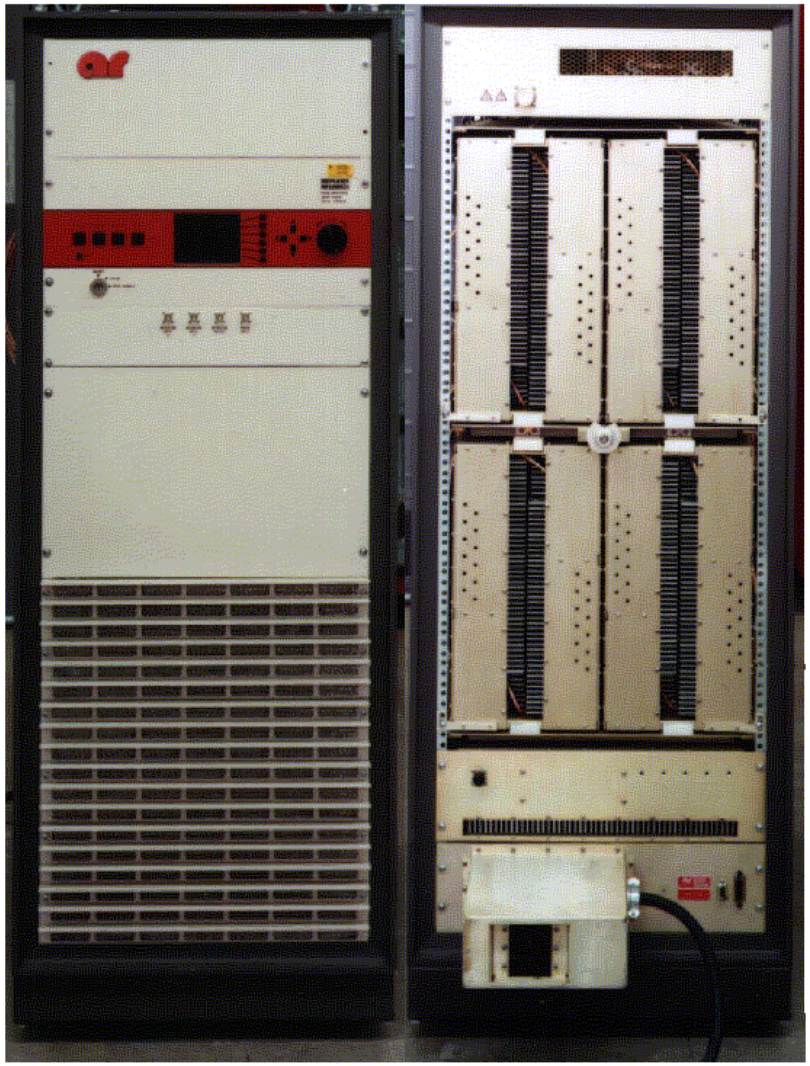
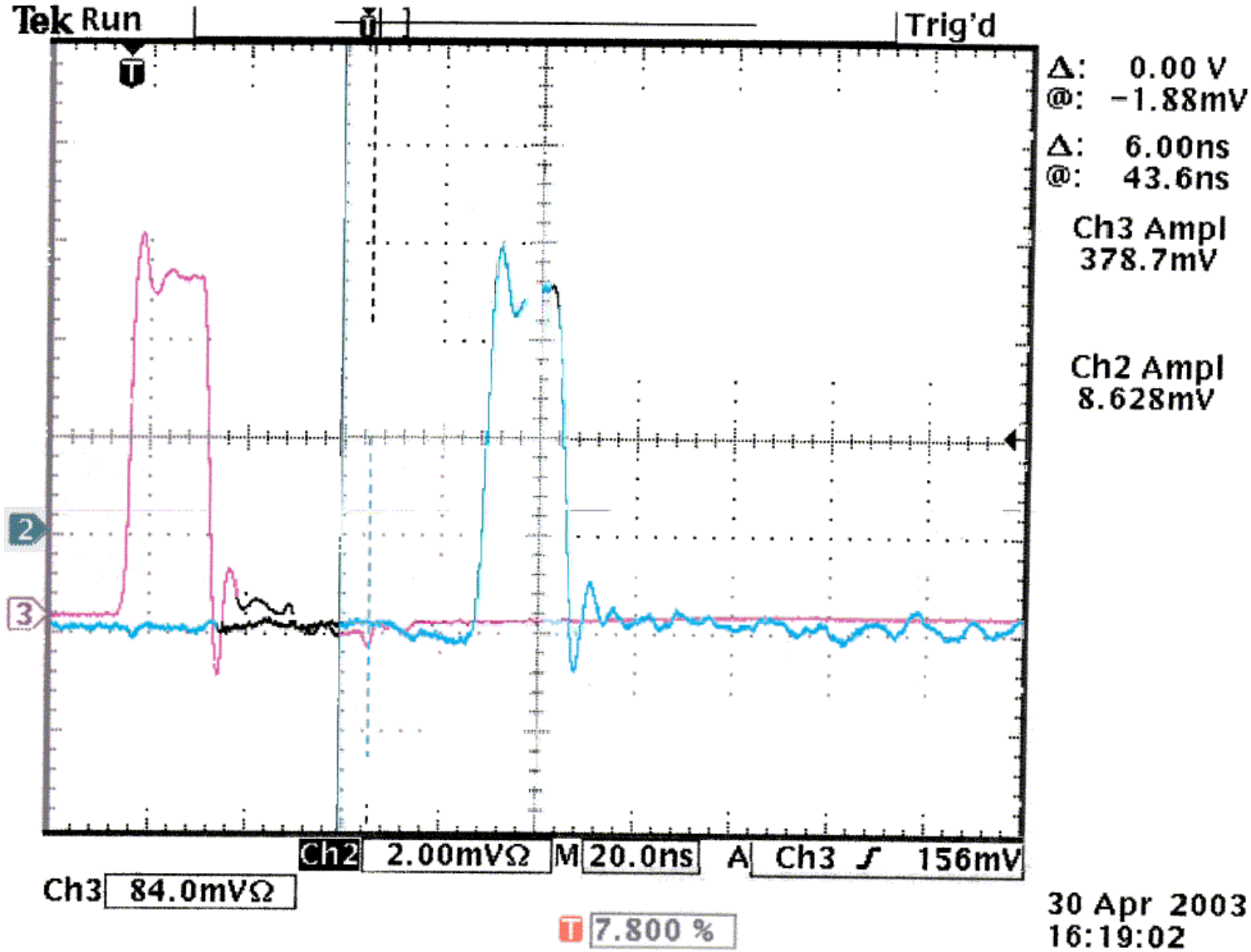


Figure 2: Front and Rear views of Amplifier Research model 3500A100.

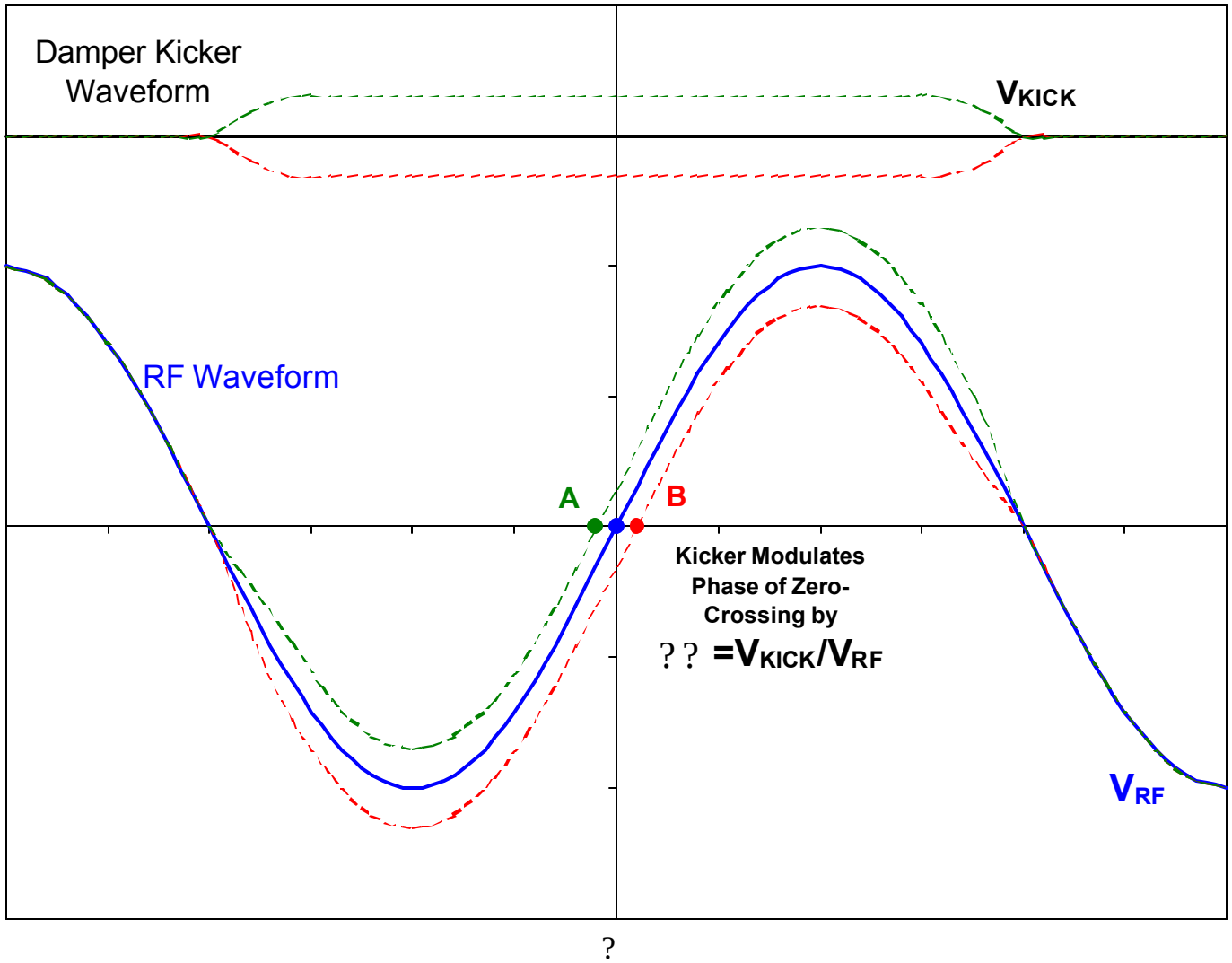
- Recycler has four of these amps (&spare), capable of generating +/-2400V or arbitrary waveform.
- MI (D. Wildman) ordered 3 more for longitudinal Dampers, *(2/3 onsite, 1 shipping ~ end july)*

✍ ~1800V of broadband voltage in MI

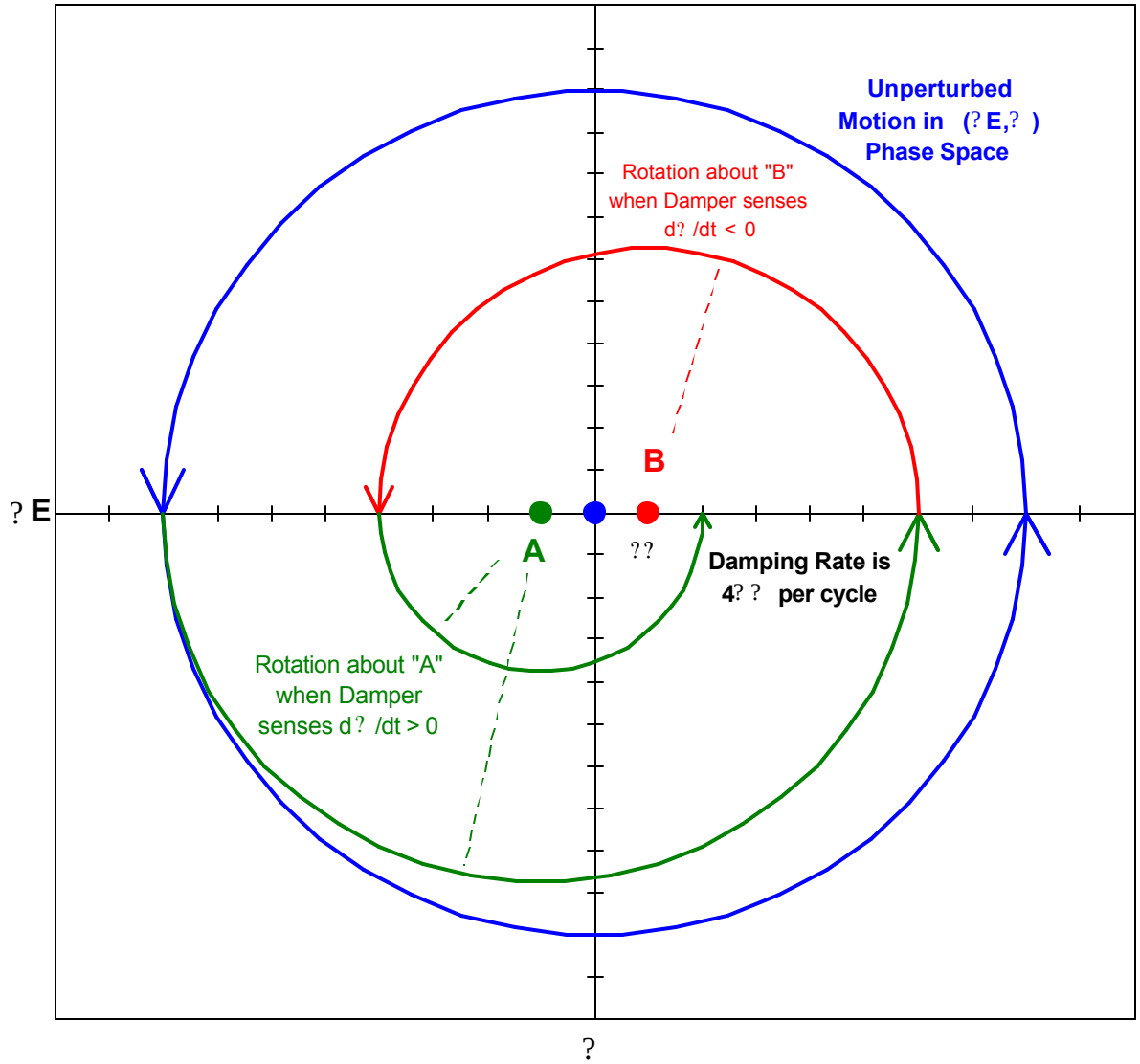
Amp & Cavity Should Give Clean 20ns Kick



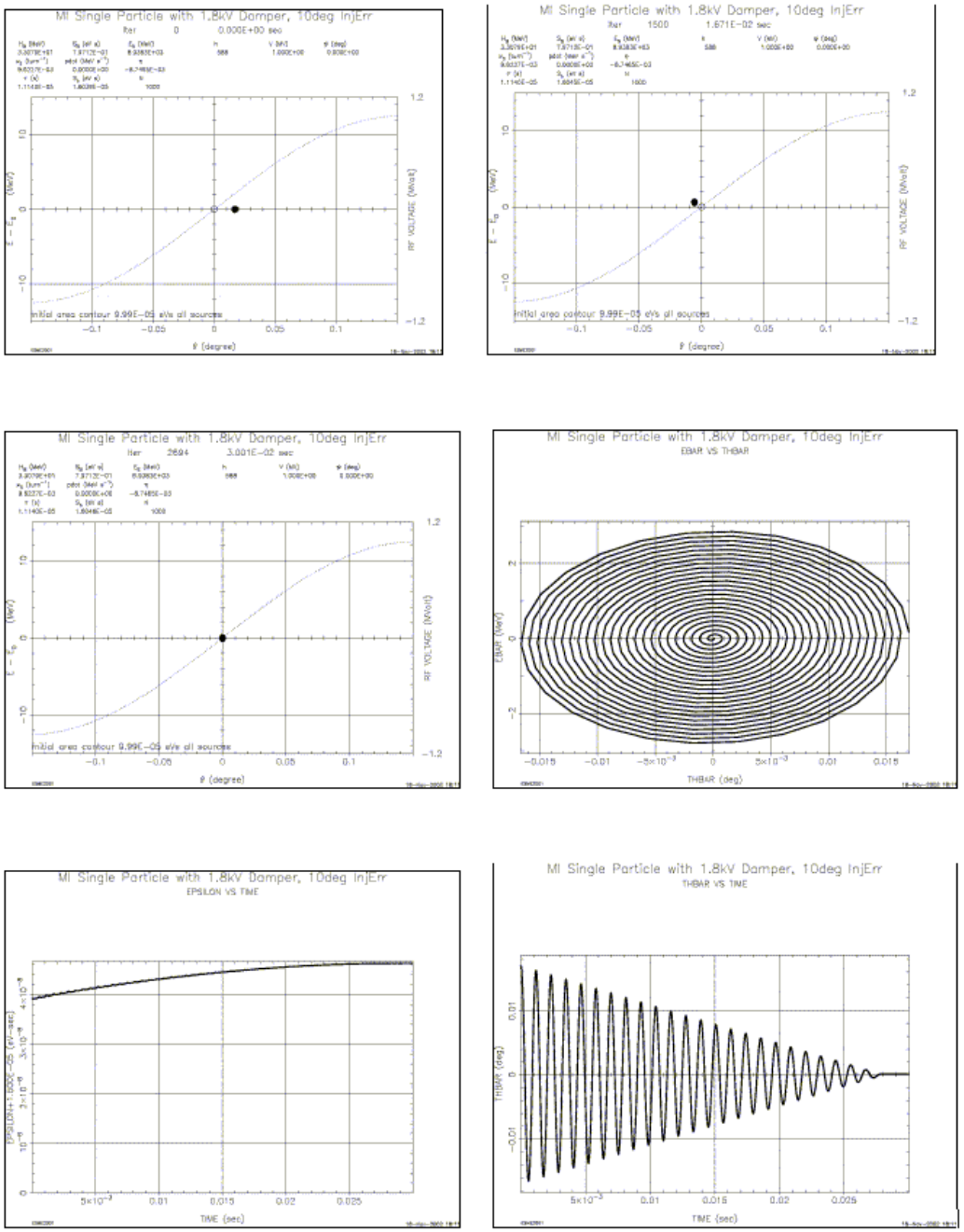
Longitudinal Damper Works by Modulating Phase of RF Zero Crossing



Damping of Bunch Motion by Modulation of Center of Rotation (RF zero-crossing) on Alternate Half-cycles of Synchrotron Motion



Longitudinal Damper Acting on a single Particle

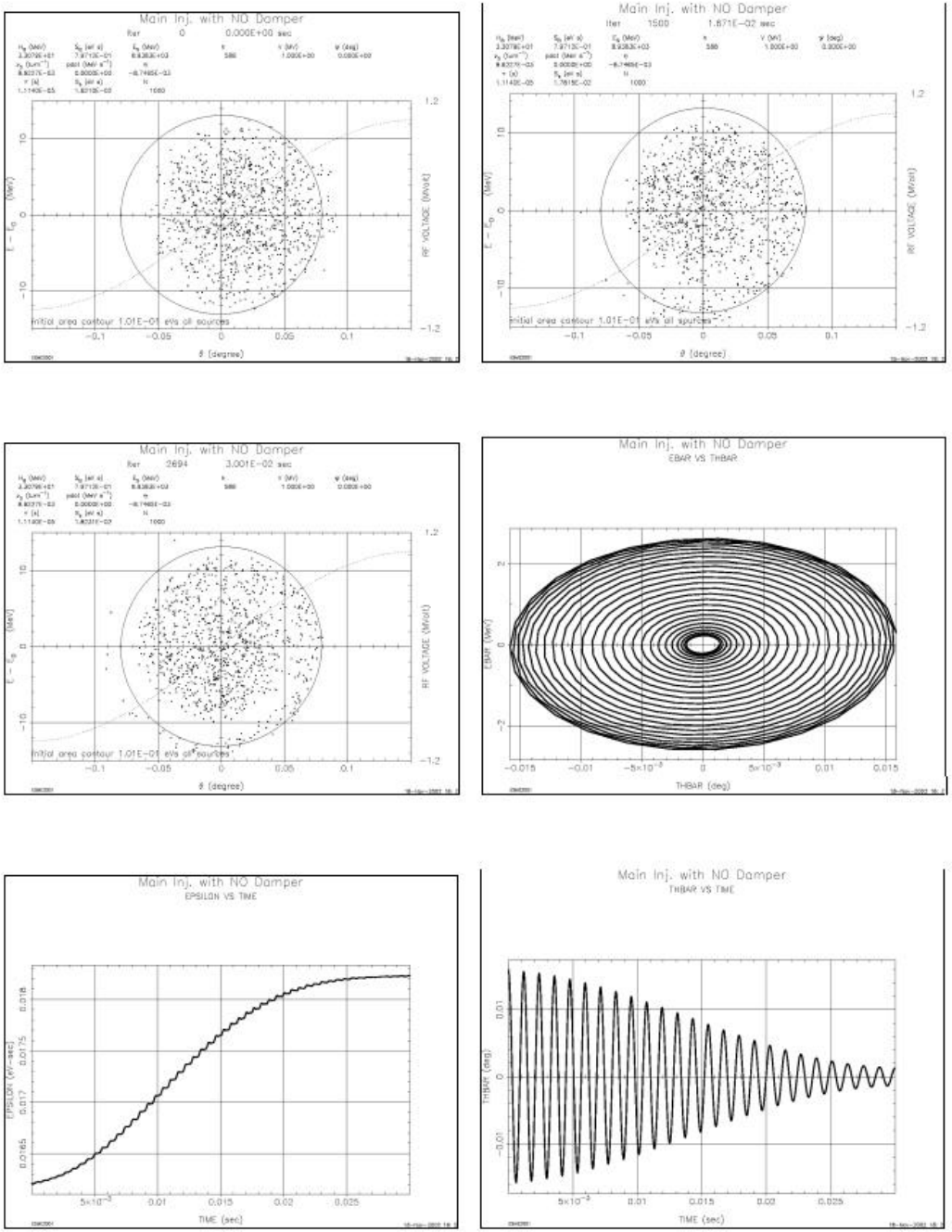


- Centroid Oscillation is driven linearly to zero.
- Damping time depends on magnitude of injection error, and damper kick voltage

CASE #1 – "Single Particle" damping with 1.8kV damper and 0.5ns initial phase error

Y. Foster

Natural Decoherence of a Single Bunch

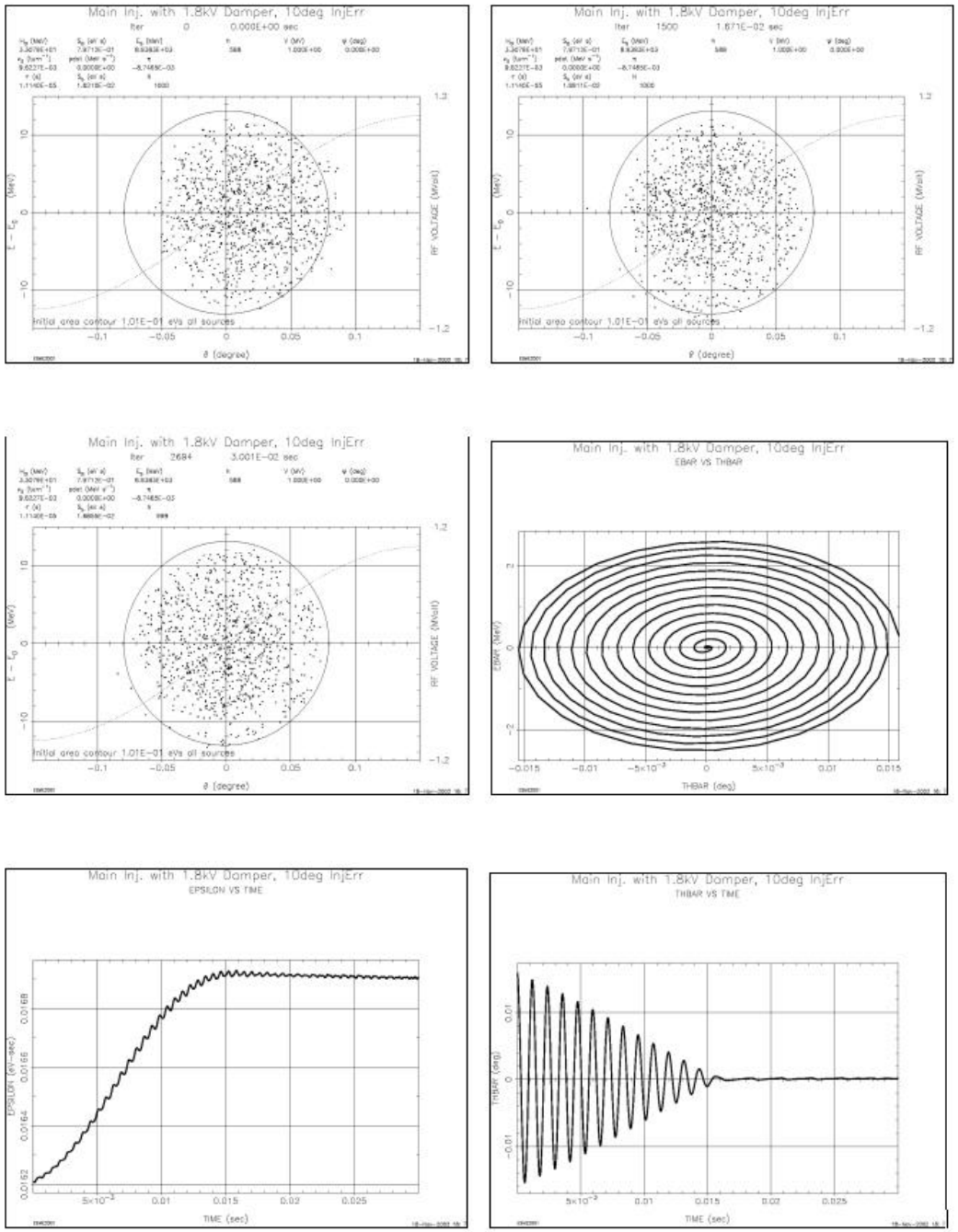


CASE #3 – Filamentation of 0.1eV-sec paraboloic bunch with no damper and 0.5ns initial phase error

- Centroid Oscillation "damps" naturally to zero.
- Natural damping is accompanied by emittance growth

Foster

Damping + Decoherence



CASE #2 – Damping of 0.1eV-sec paraboloic bunch with 1.8kV damper and 0.5ns initial phase error

- Centroid Oscillation is driven more quickly to zero.
- Emittance growth is reduced.

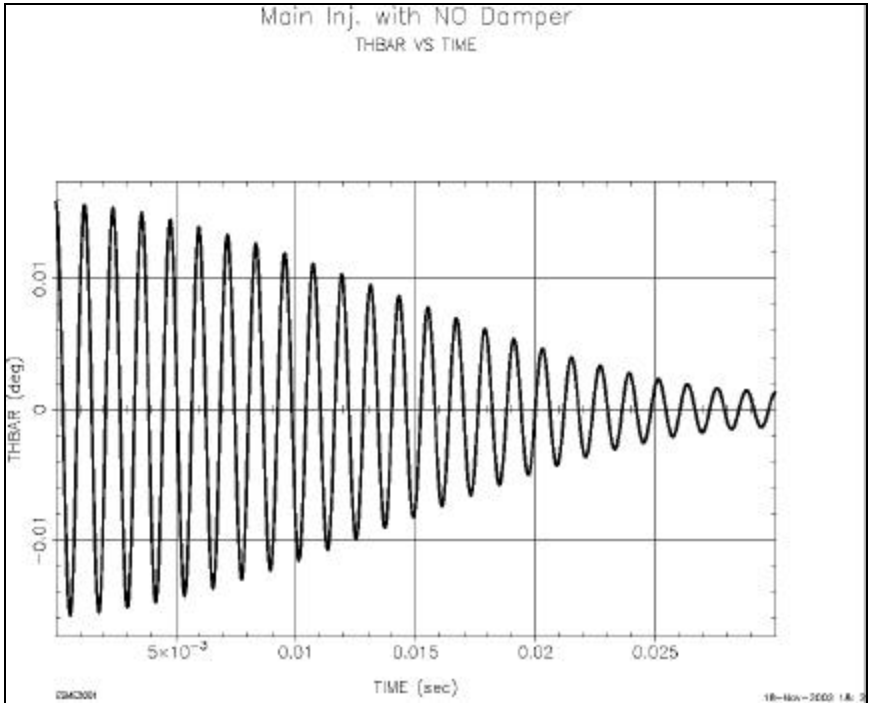
Y. Foster

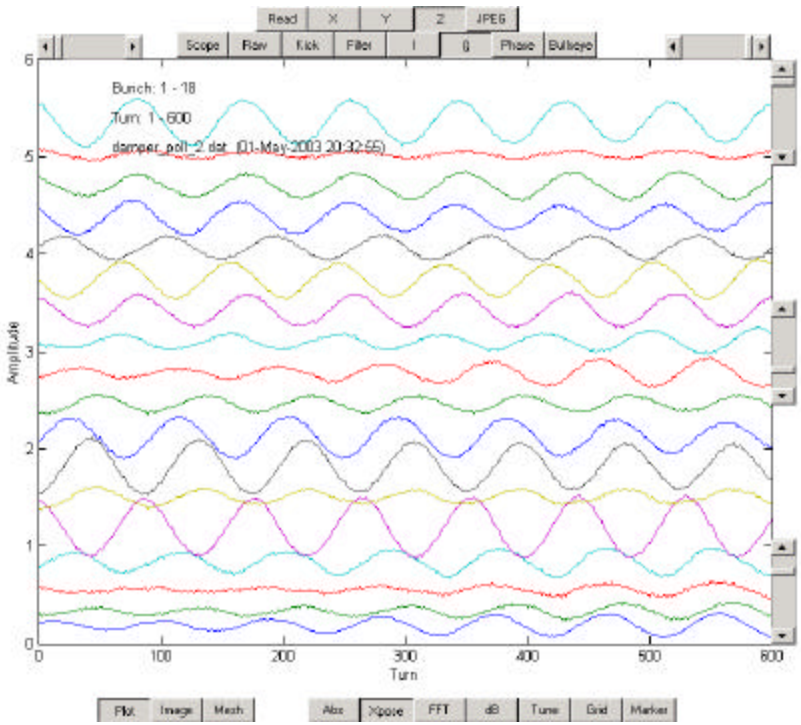
Numerical Examples for Longitudinal Dampers

	MI at Injection	Recycler
RF Voltage	1000 kV	2 kV
Damper Voltage	1.8 kV	0.05 kV
RF frequency	53.0 MHz	2.5 MHz
Zero-Crossing Shift	0.005 ns	1.592 ns
Damping Decrement	0.022 ns/osc	6.366 ns/osc
Initial Phase Err	10 deg.	10 deg.
	0.52 ns	11.1 ns
Sychrotron Freq	870 Hz	8.5 Hz
Damping Time for	24 periods	1.7 periods
10 degree phase osc.	0.028 sec.	0.205 sec.

Damping can be made faster

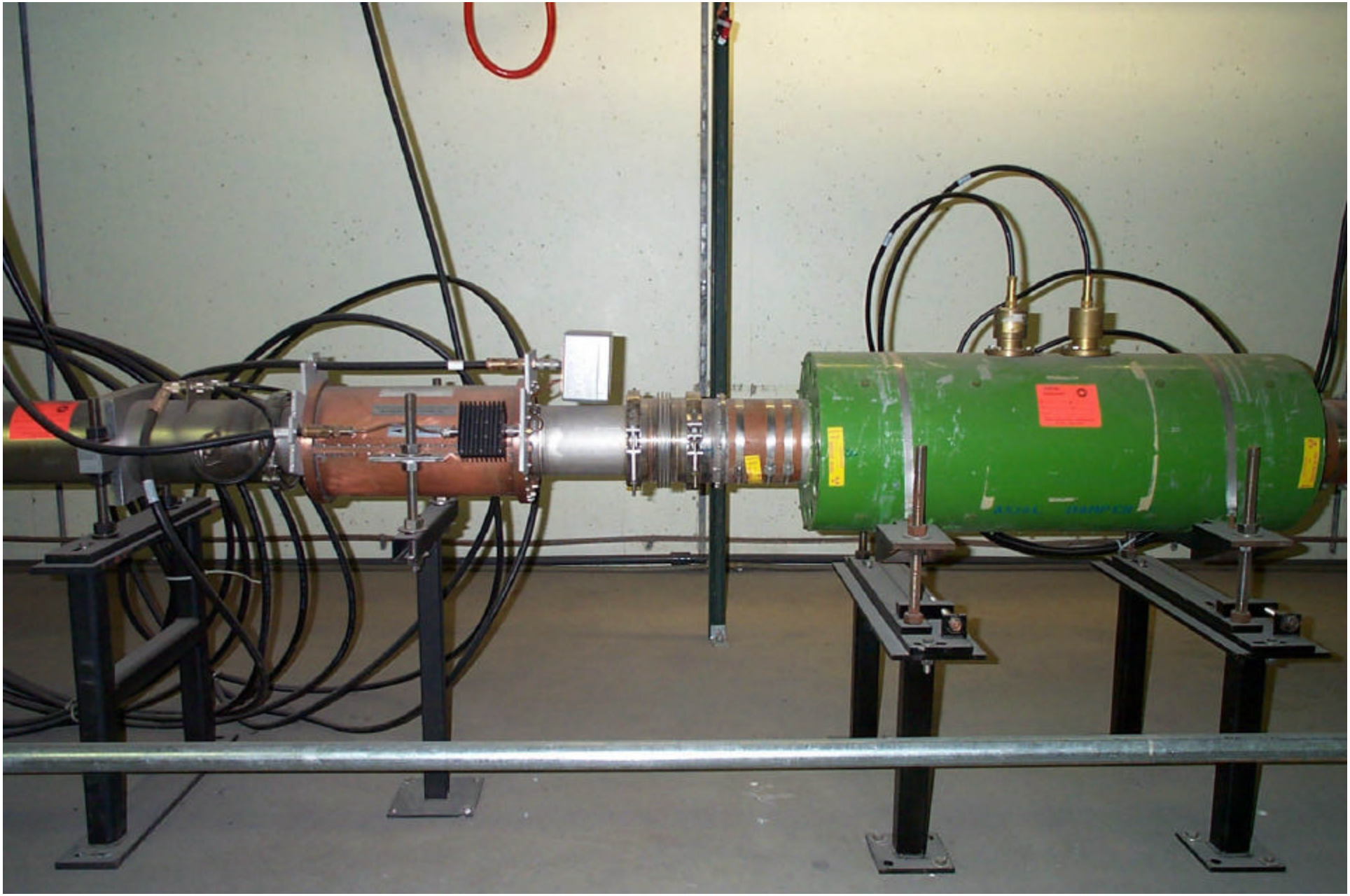
by raising V_{DAMPER} and/or lowering V_{RF}



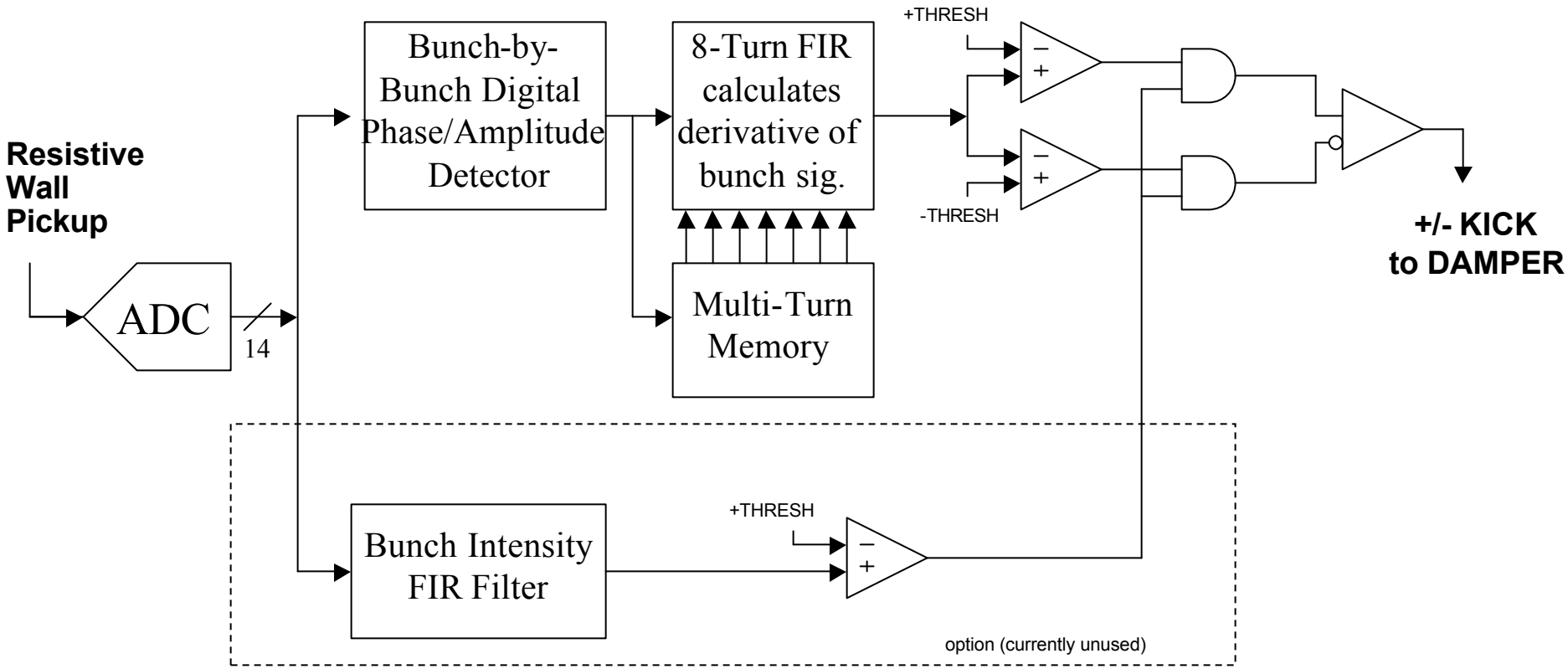


Theory & Measurement *do not agree* for longitudinal decoherence

- Longitudinal Oscillations persist for seconds to hours, (not milliseconds)!
- The worry is that megavolt-scale coherent forces frustrate longitudinal damper action.



Universal Damper FPGA Logic



Individual Bunches are kicked + or - depending on whether they are moving right or left in phase

FPGA Code for Universal Damper (8-turn Filter)

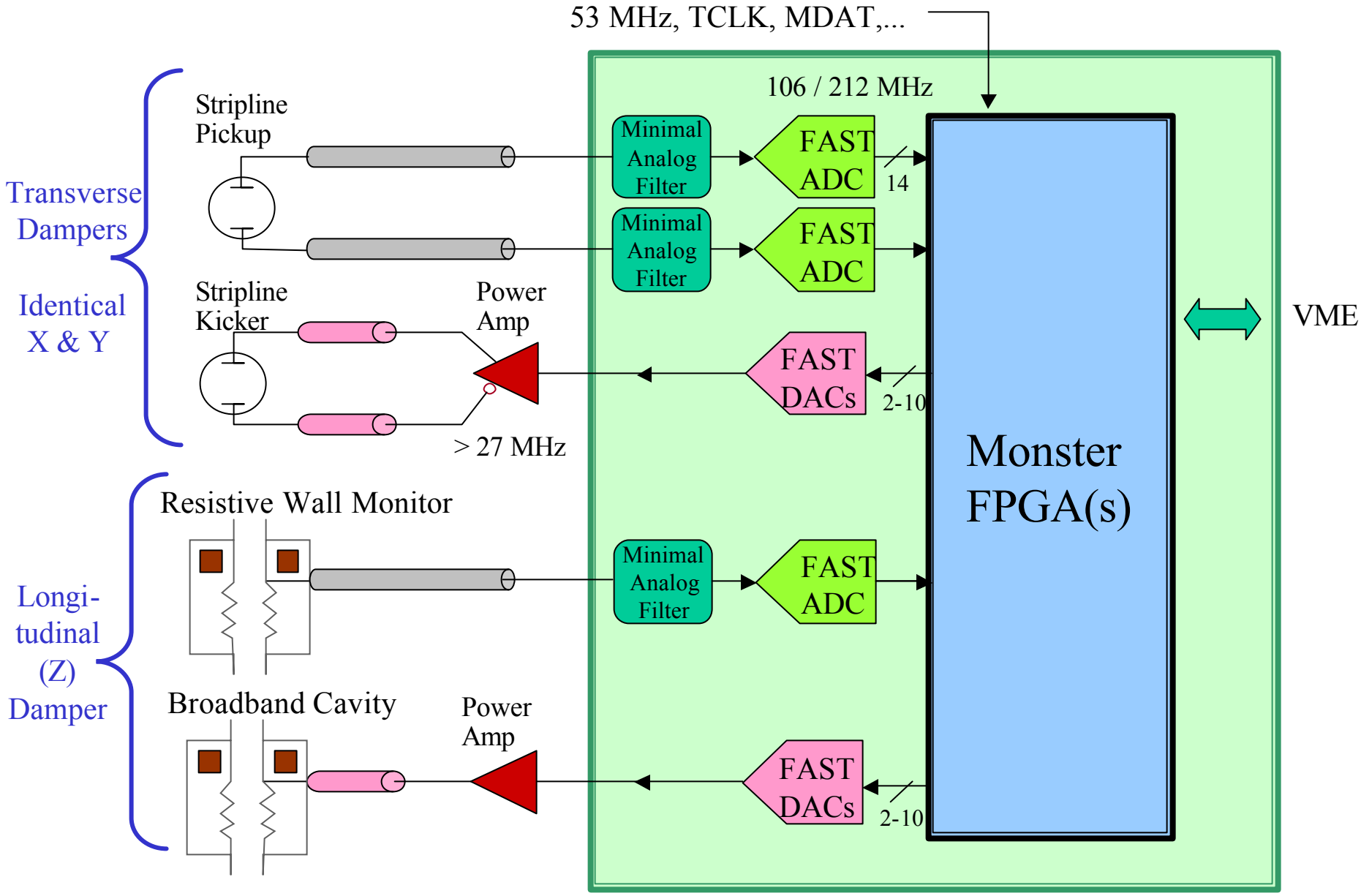
```
-- 7-Turn Delay Storage for 8-turn filter using altshift_taps megafunction (RAM-based shift register)
-------------------------------------------------------------------------------------------------------
-- shift register length between taps is Main Injector/Recycler Harmonic number (588)
()= turn_delay : altshift_taps() with (NUMBER_OF_TAPS=7, WIDTH=15,
        TAP_DISTANCE=588) returns(.taps[0]);        -- # of stages between taps = # of bunches in ring
    turn_delay.clock = adclkby2;                    -- megafunction 2-stage pipelined by 53 MHz clock
    turn_delay.shiftin[] = Qch1.q[14..0];           -- shiftreg input is Zero-turn delay signal

-- Multiply & Add pipelined megafunctions to get 8-turn weighted sum for FIR filter
-----------------------------------------------------------------------------------
-- Four multipliers and adders in each pipelined megafunction, two megafunctions for 8 total multipliers
-- first multiplier/adder for turns n,n-1,n-2,n-3
()= Mpy_Add :   altmult_add()       with (NUMBER_OF_MULTIPLIERS=4, WIDTH_A=15, WIDTH_B=4, WIDTH_RESULT=21,
                                          REPRESENTATION_A="SIGNED",REPRESENTATION_B="SIGNED",
                                          INPUT_REGISTER_A0="CLOCK0",INPUT_REGISTER_A1="CLOCK0",
                                          INPUT_REGISTER_A2="CLOCK0",INPUT_REGISTER_A3="CLOCK0",
                                          INPUT_REGISTER_B0="CLOCK0",INPUT_REGISTER_B1="CLOCK0",
                                          INPUT_REGISTER_B2="CLOCK0",INPUT_REGISTER_B3="CLOCK0")
                                    returns(.result[0]);    -- 1-bit dummy, actually returns nothing
    Mpy_Add.datab[15..0]    = FIR_coeffs[15..0];        -- multiply by four 4-bit signed numbers from VME control registers
    Mpy_Add.dataa[14..0]    = Qch1.q[14..0];            -- zero turn delay is multiplier port A0
    Mpy_Add.dataa[59..15]   = turn_delay.taps[44..0];   -- 1,2, and 3 turn delays are multiplier ports A1,A2,A3
    Mpy_Add.clock0  = adclkby2;                         -- pipelined result comes out 3 clocks later

-- second multiplier/adder for turns n-4,n-5,n-6,n-7
()= Mpy_Add2    :   altmult_add()       with (NUMBER_OF_MULTIPLIERS=4, WIDTH_A=15, WIDTH_B=4, WIDTH_RESULT=21,
                                          REPRESENTATION_A="SIGNED",REPRESENTATION_B="SIGNED",
                                          INPUT_REGISTER_A0="CLOCK0",INPUT_REGISTER_A1="CLOCK0",
                                          INPUT_REGISTER_A2="CLOCK0",INPUT_REGISTER_A3="CLOCK0",
                                          INPUT_REGISTER_B0="CLOCK0",INPUT_REGISTER_B1="CLOCK0",
                                          INPUT_REGISTER_B2="CLOCK0",INPUT_REGISTER_B3="CLOCK0")
                                    returns(.result[0]);    -- 1-bit dummy, actually returns nothing
    Mpy_Add2.datab[15..0]   = FIR_coeffs[31..16];       -- multiply by four 4-bit signed numbers from VME control registers
    Mpy_Add2.dataa[59..0]   = turn_delay.taps[104..45]; -- 4,5,6, and 7 turn delays are multiplier ports A0,A1,A2,A3
    Mpy_Add2.clock0 = adclkby2;                         -- pipelined result comes out 3 clocks later

-- Add Damper results of both Multiply/Add megafunctions to get final result for 8-turn weighted sum
()= mpySum  : lpm_add_sub() with (lpm_width=22, lpm_direction="add") returns (.cout);
    mpySum.dataa[20..0]     = mpy_add.result[20..0];        -- add result of first four multipliers
    mpySum.dataa[21]        = mpy_add.result[20];           --      (sign extend)
    mpySum.datab[20..0]     = mpy_add2.result[20..0];       -- add result of second four multipliers
    mpySum.datab[21]        = mpy_add2.result[20];          --      (sign extend)
-- Output Register for calculated kick sum
()= DK: lpm_ff (.data[] = mpySum.result[], .clock = adclkby2) with (lpm_width=22) returns (.q[0]);
```

All-Coordinate Digital Damper



New Damper Board (A. Seminov)

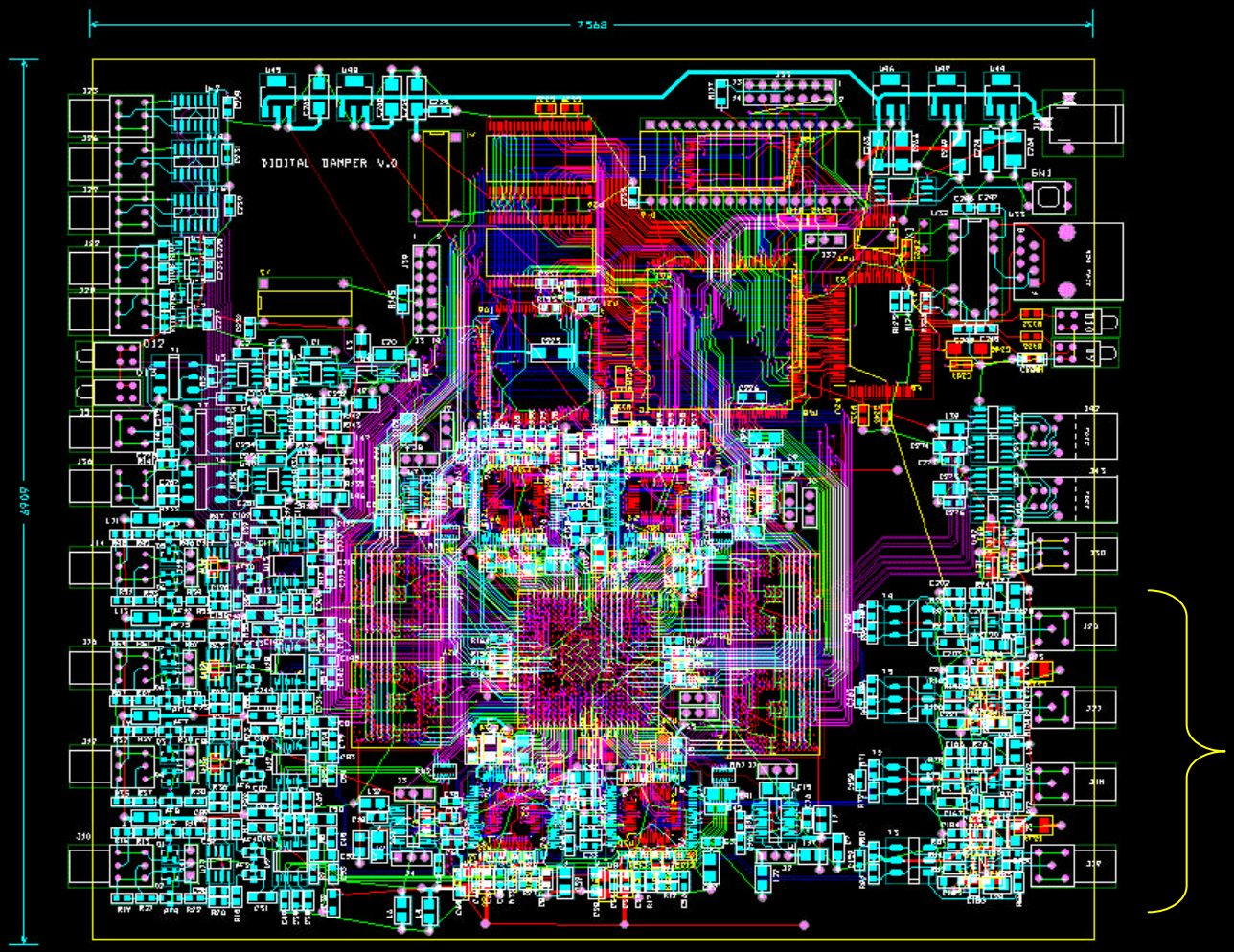
- *SINGLE* high-end FPGA (vs. 5 on Echotek)
- Four 212 MHz ADCs (vs. 106 MHz on Echotek)
- Four 424 MHz DACs (vs. 212 MHz on Echotek)
- Digital Inputs:
  - TCLK, MDAT, BSYNCH, 53 MHz, Marker
- Digital Outputs:
  - Pbar/P TTL, scope trigger, 1 GHz serial Links..
- "NIM module" with Ethernet interface to ACNET

Layout Plus -- D:\BEAMS\GWF\DDAMPER\DAMPER_LVDS_V1.MAX

File Edit View Tool Options Auto Window Help

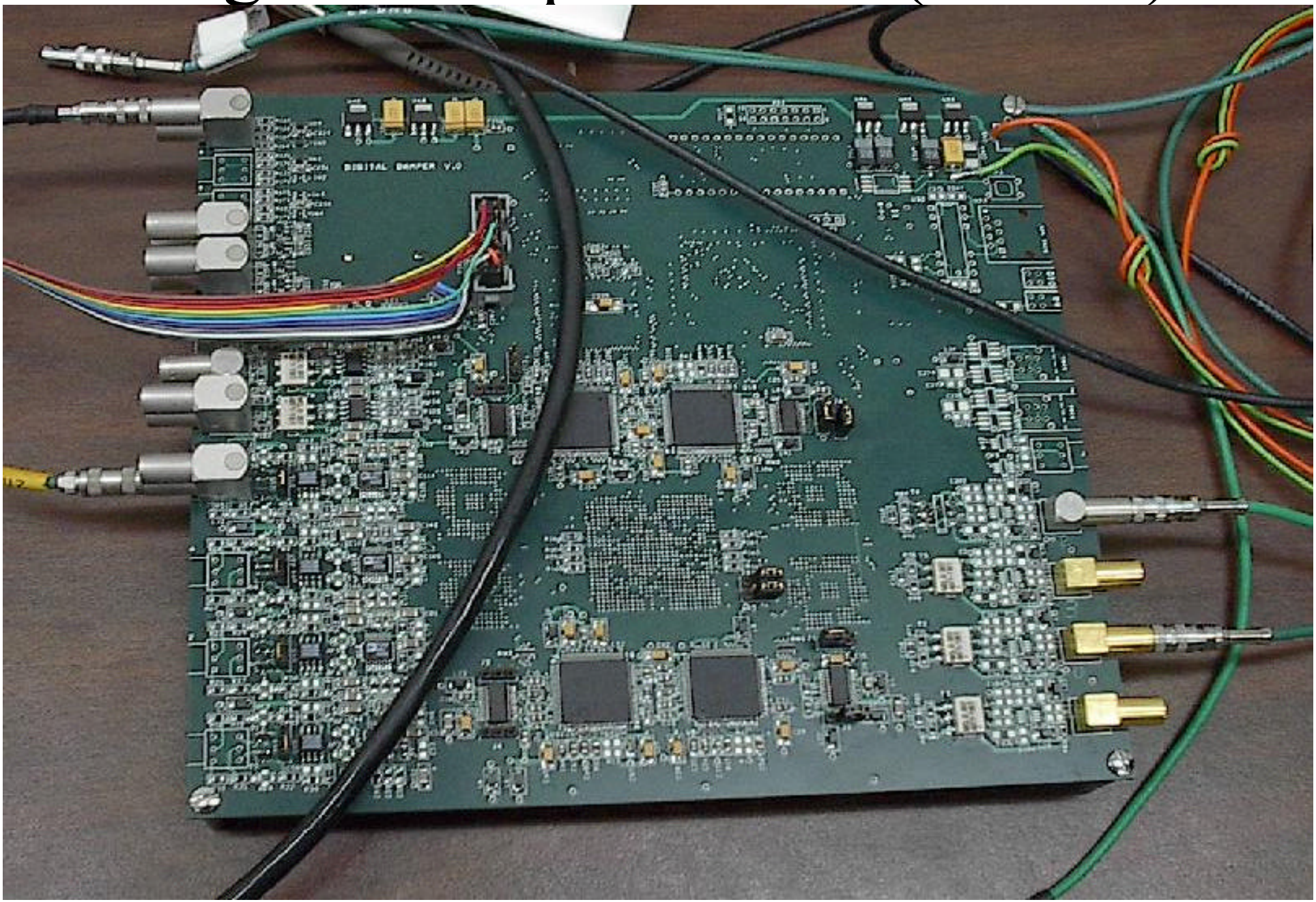
X 2320 Y 4616 G 8 16 I12

Design - Component (DRC OFF)



[2320,4616] RAM: 5438K Used, 1054076K Available

Digital Damper Board (~ NIM)



ACNET CONTROLS

- Damper must behave differently for different bunches ==> bunch-by-bunch RAM
  - Specifies Damper Gain, anti damp, noise injection, pinging, etc. on bunch-by-bunch basis.
- Damper must behave differently on different MI cycles
  - Each control register becomes an ACNET Array Device indexed by MI State
  - Register contents switch automatically when MI State changes *(D. Nicklaus)*

ACNET Control Devices (>250 total)

```
PA:I34 INT MON PARAM<NoSets>
I34                                  SET     D/A   A/D  Com-U *COPIES*
-<FTP>+ *SA+ X-A/D  X=TIME     Y=E:DYR01G,E:DYR02G,E:DTS01G,E:DTS02G
COMMAND ---- Volts  I= 0       I= 475.16 , 473.9  , 303.2  , 303.47
-< 1>+  One+ AUTO   F= 600     F= 475.19 , 473.93 , 303.23 , 303.5
fbi.... sbd.... 8gev... ibeam's tune... ipm.... toroid  DAMPERS
-I:DDCMSS     Damper MI State Selec  0          0
 ! DIGITAL DAMPER MAIN CONTROLS
 ! ---------------------------

 ! MASTER ENABLE SWITCH   1=ON, 0=OFF
-I:DDCPWR     Damper On/Off Switch   0          0         1=on

 ! MI STATE SELECT (SINGLE USER)
 !
-I:DDCMSS     Damper MI State Selec  0          0
 I:DDCMIS     Damper MDAT MI State              3

 ! DAMPER ENABLE/MUTE [0:30]  0=OFF, 1=MUTE, 2=ON
-I:DDXDEN     X Dampr Enable/Mute    0          0
-I:DDYDEN     Y Dampr Enable/Mute    0          0
-I:DDZDEN     Z Dampr Enable/Mute    0          0

 !DAMPER ACTIVE VARIABLE
 I:DDXACT     X Dampr Active                    0
 I:DDYACT     Y Dampr Active                    0
 I:DDZACT     Z Dampr Active                    0

 ! BEAM RF STRUCTURE DAMPER IS EXPECTING
-I:DDXRFT     X Dampr RF Type        0          0
-I:DDYRFT     Y Dampr RF Type        0          0
-I:DDZRFT     Z Dampr RF Type        0          0

-I:DDXDEN[3]  X Dampr Enable/Mute    0          0
-I:DDXDEN[25] X Dampr Enable/Mute    0          0

-I:DDYDEN[3]  Y Dampr Enable/Mute    0          0
-I:DDYDEN[25] Y Dampr Enable/Mute    0          0

-I:DDZDEN[3]  Z Dampr Enable/Mute    0          0
-I:DDZDEN[25] Z Dampr Enable/Mute    0          0
Java Applet Window
```

- Master control registers & diagnostics are typically single devices
- Configuration control registers are array devices indexed by MI State

Adding a new ACNET Device

1) Add register(s) to FPGA Firmware

```
-- TEST DEVICE     -- captures Damper Filter output for bucket #23 for Fast-Time Plot

IF (dsel.q & addr[]==H"0088") THEN          -- VME Address decode
    datatri[]= lpm_ff(                      -- connect register to VME read data bus
        .clock  =   adclkby2,               -- clocked at 53 MHz
        .enable =   Bucket_Count==23,       -- clock enabled when RF bucket counter=23
        .data[] =   Filter_Out_32_bit[])    -- data from filter output
        with (LPM_WIDTH=32);                -- register is 32 bits wide
END IF
```

2) Start Recompile (takes ~6 minutes)

3) Meanwhile, use DABBEL/D80 to define properties of new ACNET device

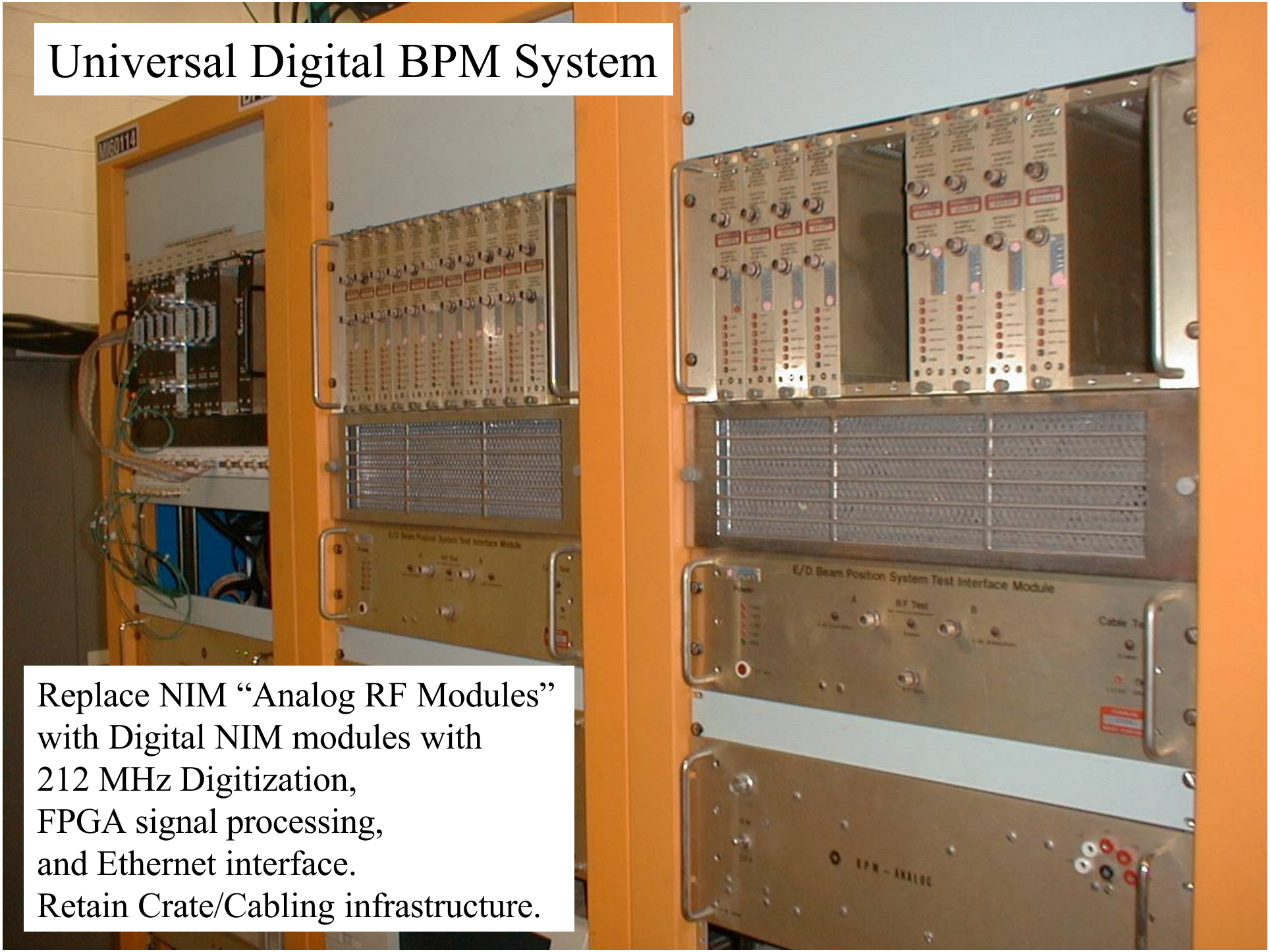
4) Download Firmware & Reboot Crate (~2 min.)

- *Takes about 10 minutes from concept to Fast-Time Plot of new ACNET variable*

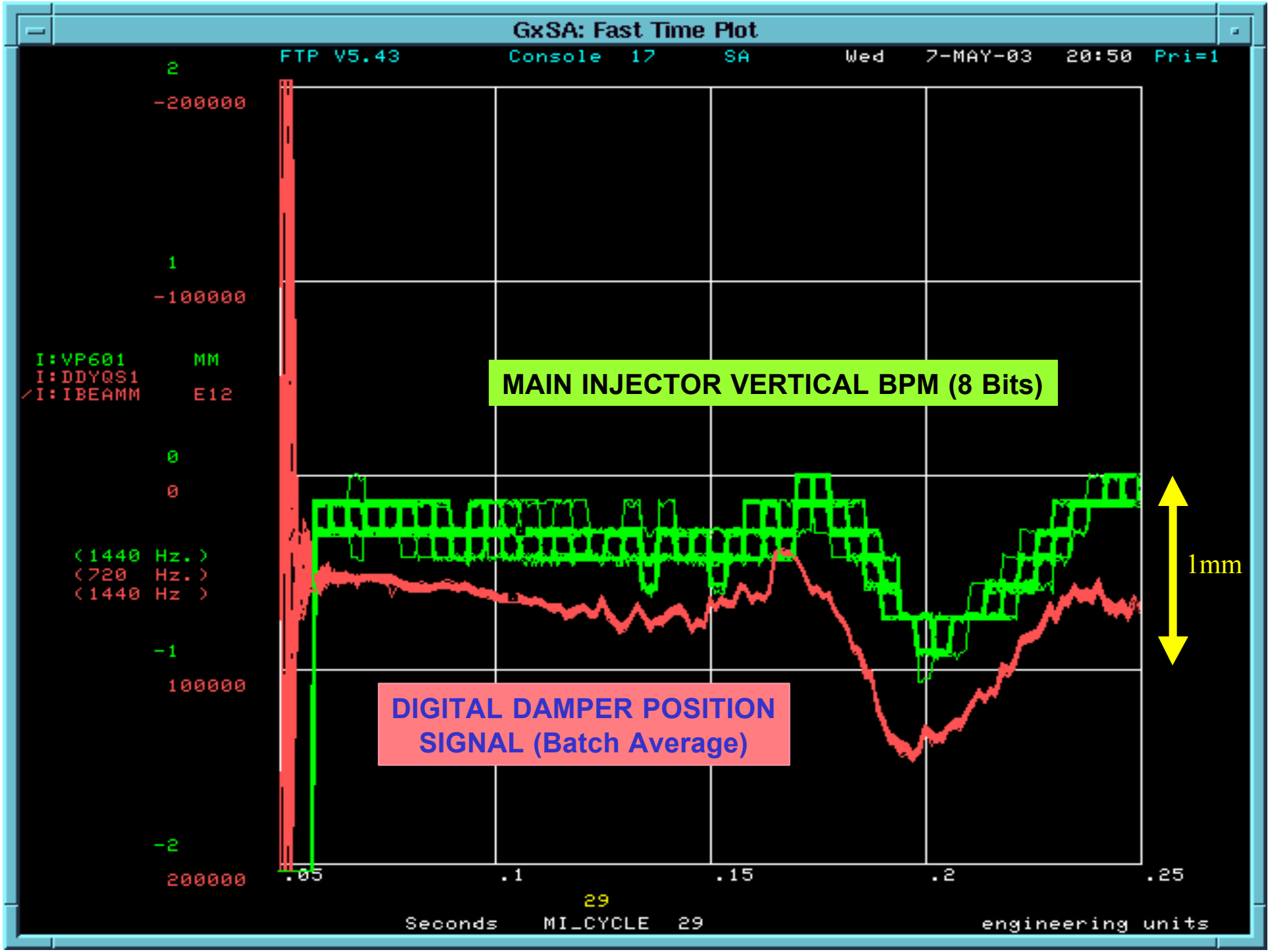
Other Applications of this Digital/FPGA Hardware Approach

- Booster Damper w/identical hardware
- Universal BPM System
- Generic Instrumentation with shared Hardware/Software infrastructure
- God's Own Beam Loading Compensation
- Replacing Booster LLRF with one "Digital NIM" module

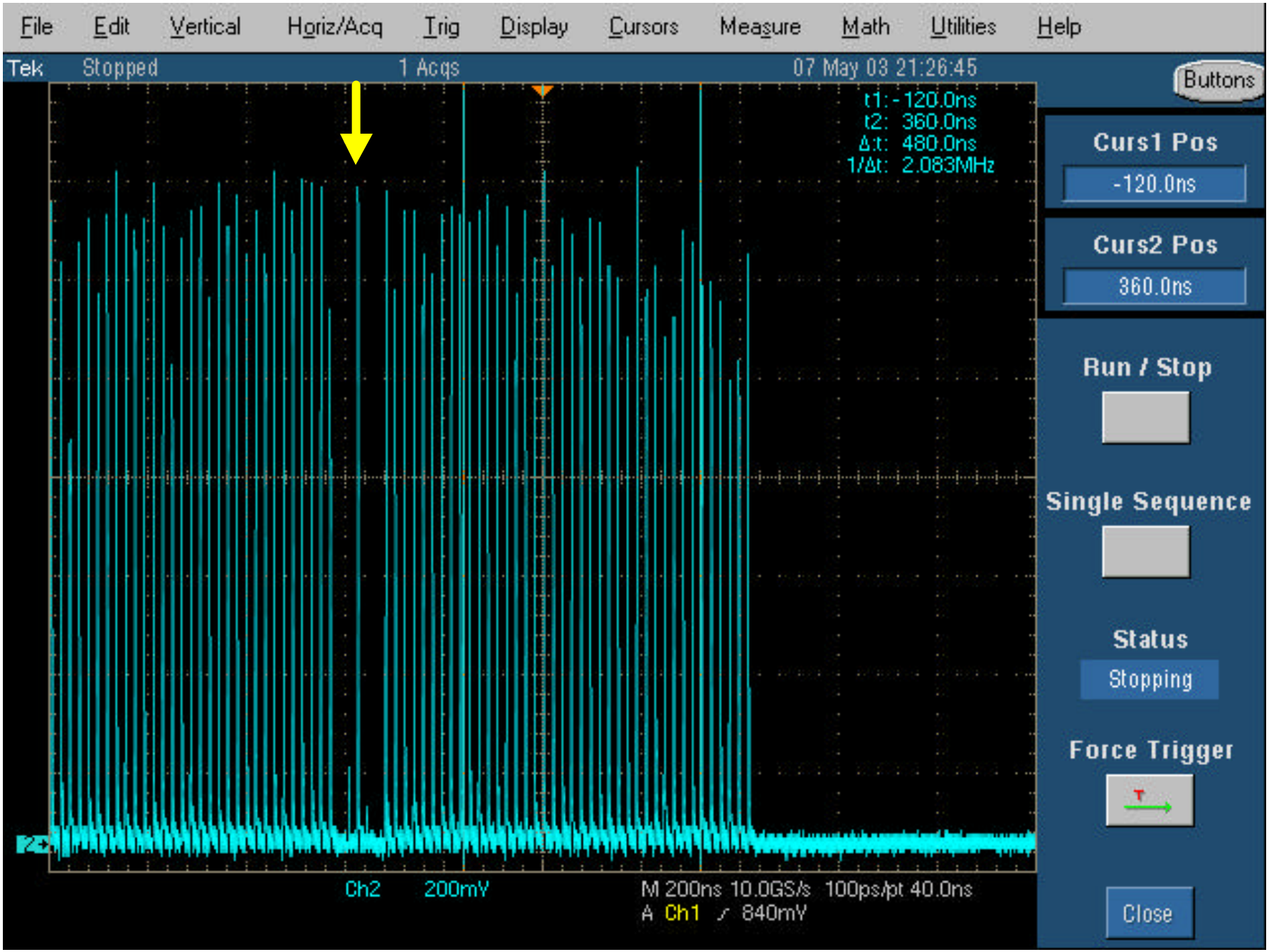
Universal Digital BPM System

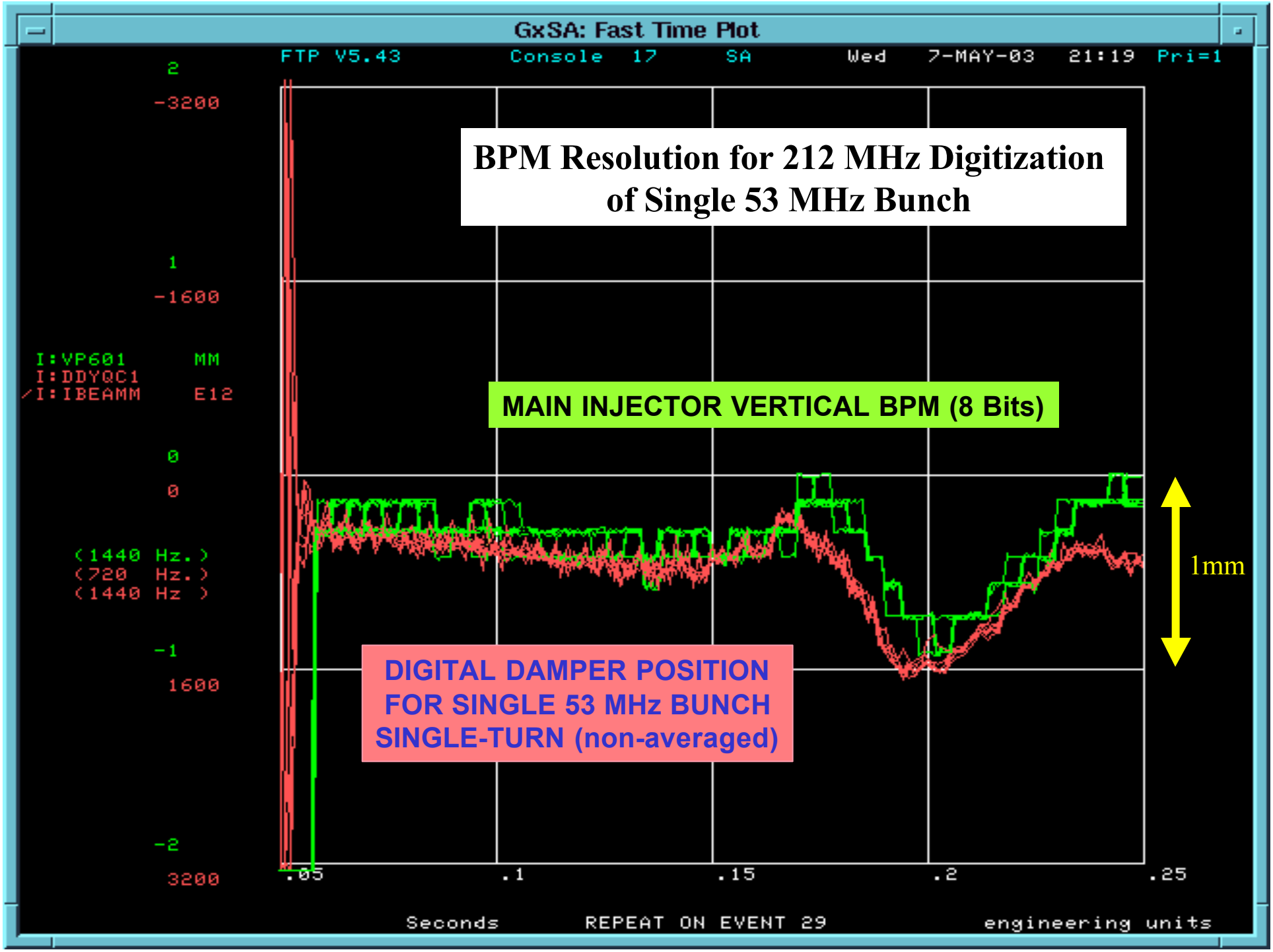


Replace NIM “Analog RF Modules”
with Digital NIM modules with
212 MHz Digitization,
FPGA signal processing,
and Ethernet interface.
Retain Crate/Cabling infrastructure.


GxSA: Fast Time Plot
FTP V5.43
Console 17
SA
Wed 7-MAY-03 20:50 Pri=1
2
-200000
1
-100000
I:VP601 MM
I:DDYQS1
/I:IBEAMM E12
0
0
(1440 Hz.)
(720 Hz.)
(1440 Hz)
-1
100000
-2
200000
.05
.1
.15
.2
.25
29
Seconds MI_CYCLE 29
engineering units
MAIN INJECTOR VERTICAL BPM (8 Bits)
DIGITAL DAMPER POSITION SIGNAL (Batch Average)
1mm

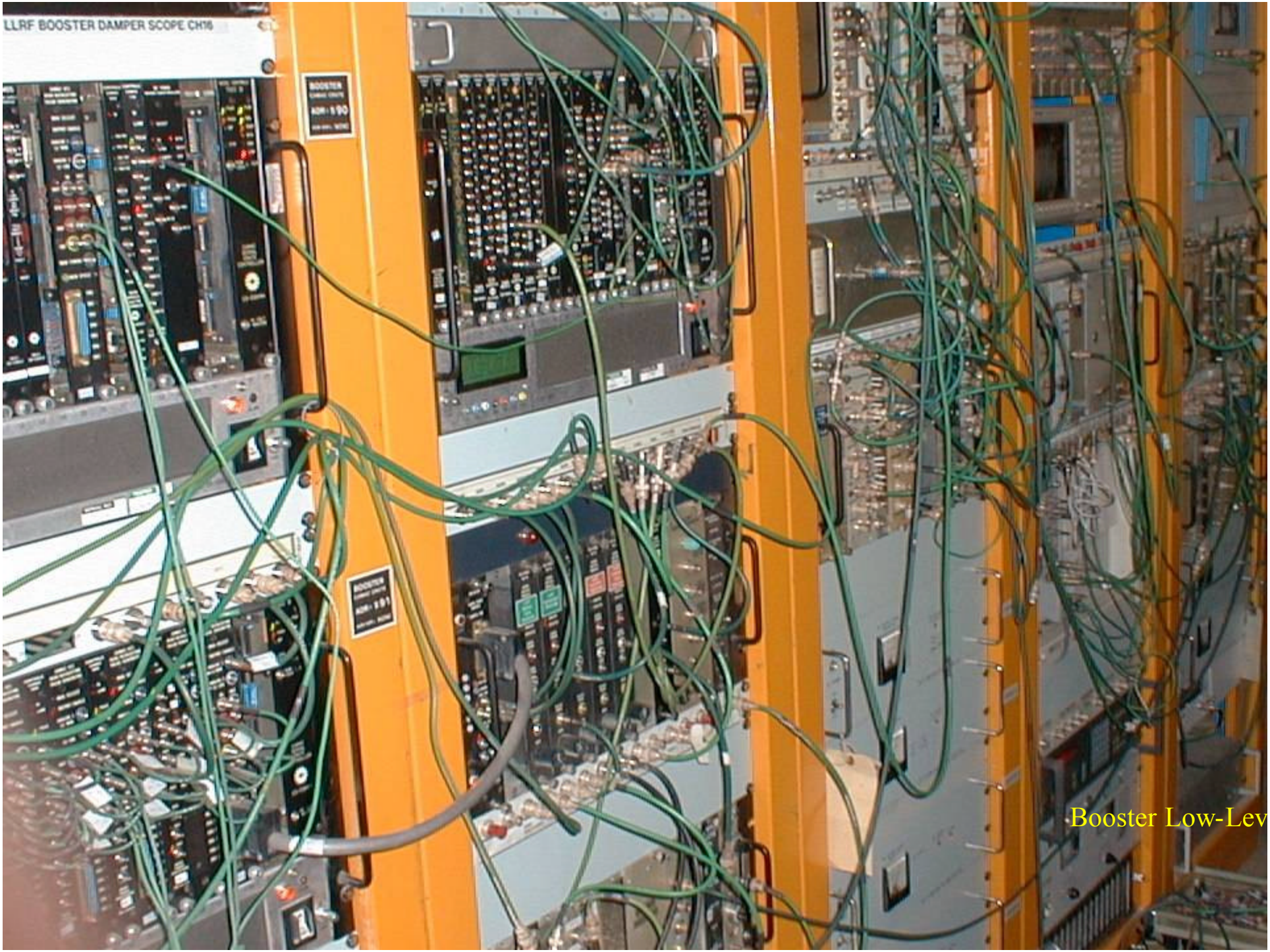
Single-Bunch BPM Measurement was tested by blowing out nearby bunches during Stacking Cycle




GxSA: Fast Time Plot
FTP V5.43
Console 17
SA
Wed 7-MAY-03 21:19 Pri=1
BPM Resolution for 212 MHz Digitization of Single 53 MHz Bunch
MAIN INJECTOR VERTICAL BPM (8 Bits)
DIGITAL DAMPER POSITION FOR SINGLE 53 MHz BUNCH SINGLE-TURN (non-averaged)
1mm
I:VP601 MM
I:DDYQC1
/I:IBEAMM E12
(1440 Hz.)
(720 Hz.)
(1440 Hz)
2
-3200
1
-1600
0
0
-1
1600
-2
3200
.05
.1
.15
.2
.25
Seconds
REPEAT ON EVENT 29
engineering units

Booster Low-Level RF.

The Final Frontier.


LLRF BOOSTER DAMPER SCOPE CH16
Booster Low-Lev