

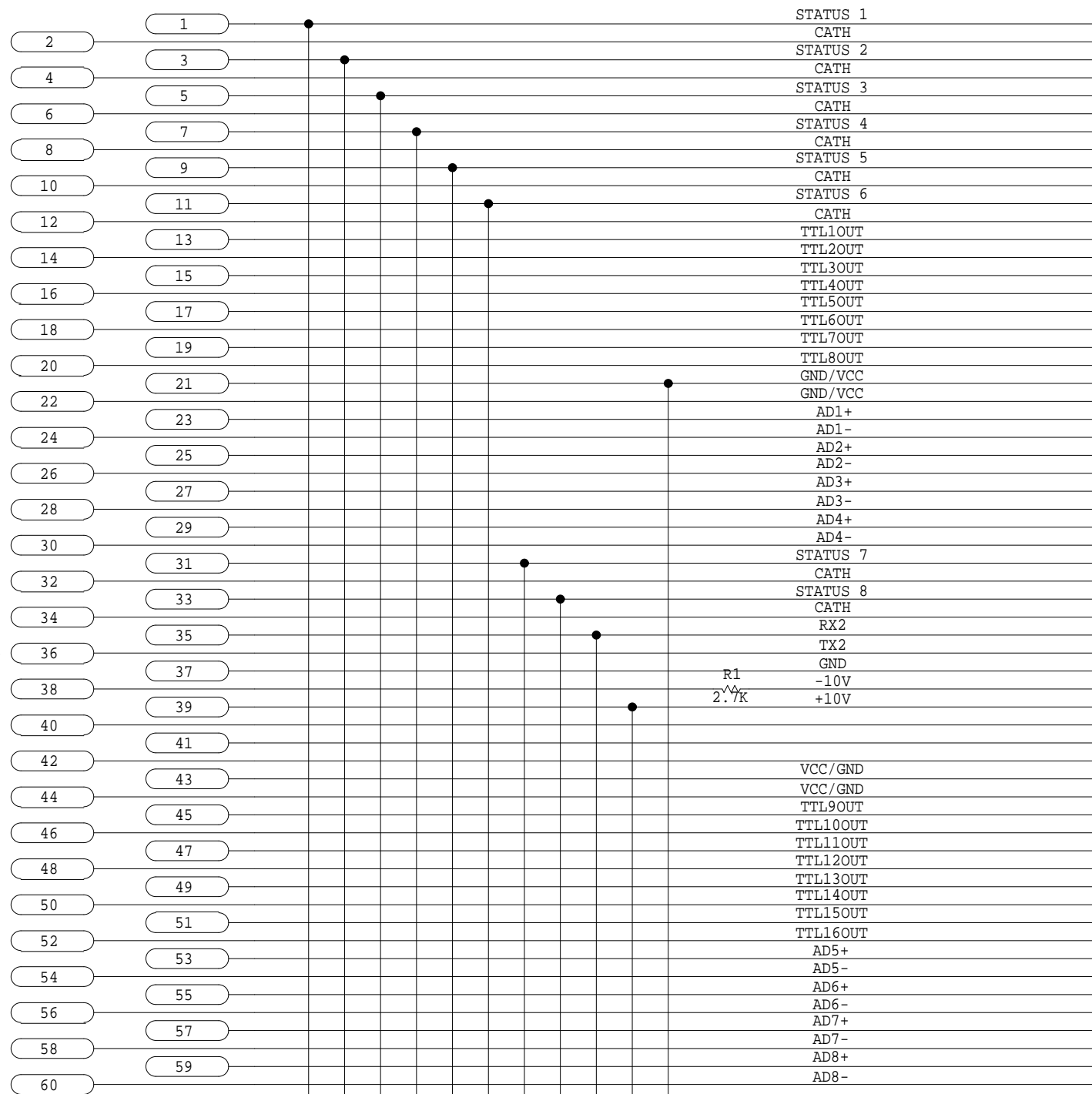
NOTES:

- Devices shown are only those used in the present configuration. For a full representation of all parts on board, see the C113 schematic(2788-ED-172877).
- Status bits are used to distinguish current usage.

Low Nibble - Bits 0 through 3	Setting
Bit 0	0 => Thermocouple
Bit 1	0
Bit 2	0
Bit 3	0
High Nibble - Bits 4 through 7	Setting
Bit 4	1 => 1200 Baud (Thermocouple Default)
Bit 5	0
Bit 6	0 => 9600 Baud (Teslometer Default)
Bit 7	0
- U18 and U19 are shown as TC5565, but can be any compatible 8K 100ns RAM. U20 and U21 are shown as 2764, but can be any compatible 8Kx8 200ns PROM.
- Switches on the I/O card are off=0, on=1

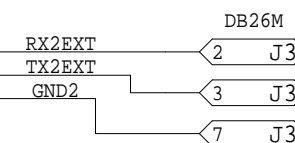
ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		ORIGINATOR	WALTER R. KNOPF 05-25-88
FRACTIONS	DECIMALS	ANGLES	DRAWN TERRY O'BRIEN 03-21-89
±	±	±	CHECKED
1. BREAK ALL SHARP EDGES 1/64 MAX		APPROVED	
2. DO NOT SCALE DWG.		USED ON	
3. DIMENSIONING IN ACCORD WITH ANSI Y14.5 STD'S.		MATERIAL	
MAX. ALL MACHINED SURFACES			

60 PIN AMP

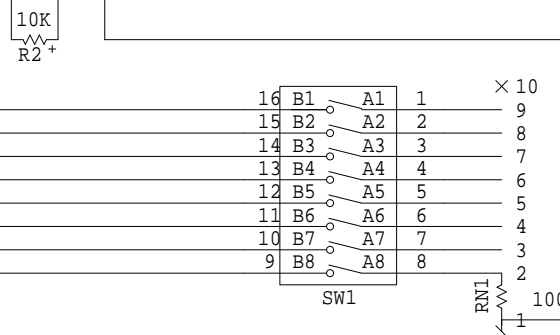


This jumpering is on the I/O card to accommodate the I/O status switches on the card. By changing the switch settings the user changes the personality of the module.
Please note that "jmp28" on the c1003 board must be installed to from 1 to 2 in order for the switch to work.

For further information see
R.D. Controls Hardware Release Note 16.0
CAMAC C1003 Module



J1



ORIGINATOR	T. O'BRIEN	4/18/89
DRAWN	C. LUNDBERG	4/18/89
CHECKED	J. GREEN	4/18/89
APPROVED		

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

RESEARCH DIVISION/CONTROLS
60 PIN I/O BOARD
C1003 I/O WIRING

SCALE	DRAWING NUMBER Warner::[hwdocs.c1003]c1003io.sch	REV. B
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