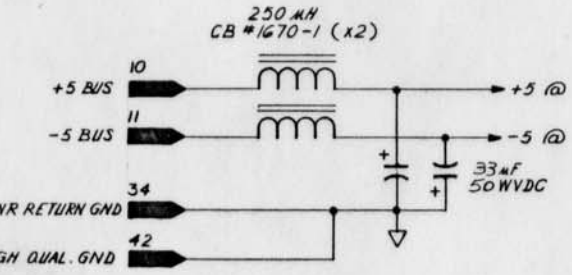


REV.	DESCRIPTION	DRAWN	DATE
A	RF PREAMP + INPUT COMPARATOR CHANGES. ADDED NOTES 5 + 6.	RJ Ducal	7-17-82
B	ADDED UR5, UR6, UR7, + UR8	RJ Ducal	9-17-82
C	ADDED UR9 + UR10, MINOR CIRCUIT MODIFICATIONS.	RJ Ducal	8-22-83
D	ADDED UR11 + UR12 AND NOTE 8.	RJ Ducal	3-11-85



REALIZED CONFIGURATIONS (CONT)

- UR9 - FAN-OUT WITH DC INPUT + OUTPUT.
- UR10 - FAN-IN WITH DC INPUT + OUTPUT.
- UR11 - FAN-OUT WITH DC INPUT, 7.5 MHz
- UR12 - FAN-OUT WITH RF INPUT PRE-AMP, 7.5 MHz

NOTES

1. ALL IC'S ARE ON SOCKETS.
2. $f_c \approx 4.8$ MHz.
3. ALL RESISTORS $\frac{1}{4}$ W 5% UOM.
4. INPUT THRESHOLD IS ADJUSTED TO +100mV FOR RF INPUTS ($R_1 = 10K$) AND TO +1V FOR DC INPUTS ($R_1 = 1.5K$).
5. S SERIES CHIPS MAY BE SUBSTITUTED FOR F SERIES CHIPS UPON CHECKOUT.
6. FOR FAN-OUT CONFIGURATIONS DO NOT INSTALL IC'S 7, 8, 12, 13, + 14. PULL-UP 8-3 TO +5V WITH 4.7K Ω .
7. UNUSED GATES HAVE GROUNDDED INPUTS.
8. FOR 7.5 MHz VERSIONS: 50, 100, 65 nsec ONE SHOTS SHOULD BE 66, 132 + 87 nsec.

REALIZED CONFIGURATIONS

- UR1 - REGULAR FAN-OUT WITH DC INPUT.
- UR2 - REGULAR FAN-OUT WITH DC OUTPUT.
- UR3 - REGULAR FAN-IN WITH DC OUTPUT.
- UR4 - REGULAR FAN-OUT WITH RF INPUT PRE-AMP + DC OUTPUT.
- UR5 - REGULAR FAN-OUT WITH RF INPUT PRE-AMP.
- UR6 - REGULAR FAN-IN WITH RF INPUT PRE-AMP.
- UR7 - REGULAR FAN-IN WITH RF INPUT PRE-AMP + DC OUTPUT
- UR8 - REGULAR FAN-IN WITH DC INPUT

PRINTED CIRCUIT BOARD	
TITLE	DWG NO.
SCHEMATIC	ED-35345
ARTWORK	BD-35346
MASTER DWG	BD-35347
ASSEMBLY DWG	BC-35592
OUTLINE DWG	B
SOLDER MASK	B
SILKSCREEN	B
PARTS LIST	BP

ITEM NO.	PART NO.	DESCRIPTION OR SIZE	QTY. REQ.
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		ORIGINATOR	ROBERT J. DUCAR
FRACTIONS		DRAWN	T. SENGMANIYONG
DECIMALS		CHECKED	RJ Ducal
ANGLES		APPROVED	RJ Ducal
±		USED ON	2-15-82
±		MATERIAL	

Fermi National Accelerator Laboratory
UNITED STATES DEPARTMENT OF ENERGY

ACCELERATOR CONTROLS
10 MEGABIT LINK-UNIVERSAL REPEATER
SCHEMATIC RF-101A

SCALE	FILMED	DRAWING NUMBER	REV.
	F2/82	0818.00-ED-35345	D

FA 7/82 FB9/82 FC9/83