LINK DRIVER
CAMAC
TSCC
TEVATRON

Controls Hardware Release No. x.0

# ARBITRATING TSCC LINK DRIVER

ED-218380 EC-218377
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October 8, 1987

## 1 INTRODUCTION

The Arbitrating TSCC Link Driver (ALD) accommodates the user with a convenient parallel interface to the serial protocol demanded by the Tevatron Serial Crate Controller (TSCC). The specifications of this unique CAMAC protocol and the TSCC are detailed in Controls Hardware Release No. 2. The ALD is an upgrade of the existing TSCC Link Driver (CHR No. 8) that allows more than a single link driver to communicate with one or more CAMAC crates interfaced by a single pair of PIOX/PIOR lines. The use of the ALD in a multi-processor environment affords better utilization of available link bandwidth. The ALD is fully compatible with the existing TSCC Link Driver and may be used as a direct replacement.

The ALD provides 10 MBit/sec parallel/serial and serial/parallel conversions, echoed data comparisons, parity generation and checking, and interpretation of the TSCC response. The details of the TSCC serial protocol are thus made transparent, in large part, to the serial link user. The link arbitration scheme employed by the ALD is also transparent to the user. The ALD provides for the efficient implementation of parallel computer interfaces. Two such interfaces, generally referred to as Link Controllers, have been developed for DEC's Unibus and Intel's Multibus. The serial connections of the ALD, PIOX and PIOR, may connect directly to the 10 MBit/sec rf link hardware to support connection to distant CAMAC crates.

The Arbitrating Link Driver is packaged as a single printed circuit board in a 3.5 inch high chassis incorporating an internal power supply. The front panel includes various test points and leds to monitor the ALD operation and a six digit diagnostic counter. The rear panel provides four pairs of PIOX and PIOR coaxial connections, two twinaxial connections for connection to upstream and downstream ALDs, and two twenty-six position ribbon connector headers for the parallel connections to the associated Link Controller.

## 2 LINK DRIVER TO LINK CONTROLLER INTERFACE

The Arbitrating Link Driver contains fourteen registers directly addressable by the controller plus additional control and status lines. All signals follow the active high equals true convention. All signals are appropriately terminated at the receiving end. The register assignments are as follows:

ALD REGISTER ASSIGNMENTS

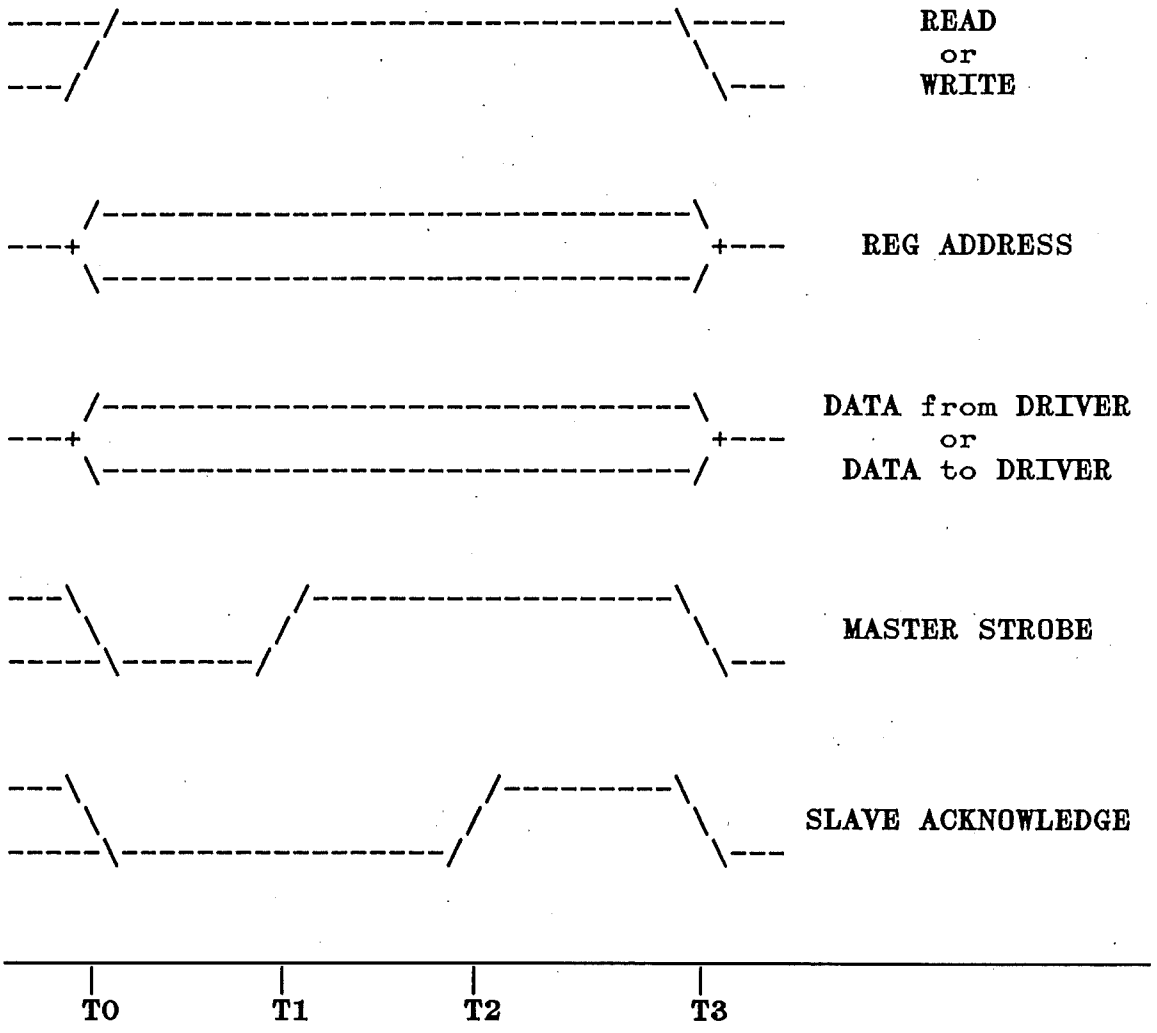
| | | |
|---|---|---|
| A(0) | R/W | Block Transfer NAF |
| A(1) | R/W | Block Transfer Word Count |
| A(2) | R/W | Block Transfer Maximum No Q |
| A(3) | R/W | Arbitration and Crate Address |
| A(4) | R/W | Programmed I/O NAF |
| A(5) | R/W | Write Data (W16 - W1) |
| A(6) | R/W | Write Data (W24 - W17) |
| A(7) | W | Trigger Serial Transmission |
| A(8) | R | Link Driver Status |
| A(9) | R | Response Data (R16 - R1) |
| A(A) | R | Response Data (R24 - R17) |
| A(B) | R | TSCC Response Status |
| A(C) | R | TSCC Response Status & Echo Crate Adr |
| A(D) | R | Echo NAF |

The register interface consists of the following:

| | |
|---|---|
| DATA | Sixteen Bi-Directional Lines D15 (MSB) thru D0 (LSB) |
| REG ADDRESS | Four Lines from Controller A4 (MSB) thru A1 (LSB) |
| READ | Line from Controller to Read Data from the Driver |
| WRITE | Line from Controller to Write Data to the Driver |
| MASTER STROBE | Line from Controller in Conjunction with Read or Write Operation |
| SLAVE ACKNOWLEDGE | Line from Driver in Response to Controller's Master Strobe |

The associated timing for register read and write operations is as follows:

## DRIVER/CONTROLLER INTERFACE TIMING




T1 = T0 + 50ns minimum  T2 = T1 + 250ns

T3 = T2 + 50ns minimum  T3 - T0 = 350ns minimum

DATA to the Driver are latched at T2.

DATA from the Driver are gated out with READ.

The fall of MASTER STROBE from the Controller causes the fall of SLAVE ACKNOWLEDGE from the Driver.

Control lines that are sourced by the Link Controller include the following:

PORT A CNTRL - When this line is asserted, the ALD is configured for Port A of the TSCC. Certain operations to the TSCC with the N(24) code are affected.

INIT - The "Initialize" line from the Controller is used to clear all circuits and sequences in the ALD. The A(0) thru A(6) registers are unaffected, but the A(8) thru A(D) registers are cleared to zero. INIT is typically generated at the beginning of a Link Driver set-up.

TRIGT - The "Trigger Transmission" line from the Controller is an alternate to the A(7) write operation for initiating the transmission of PIOX frames.

In addition to the Link Driver status provided in register A(8), a variety of directly wired status lines are made available to the Link Controller. These lines are asserted at the fall of BUSY and may be used for sequencing or as interrupts in specialized controllers. The status lines that are sourced by the Link Driver include the following:

BUSY - Indicates that a request for transmission of PIOX frames has been received. BUSY falls at the conclusion of the receipt of PIOR frames or at the assertion of TIMEOUT. For the ALD, the longest duration of BUSY assertion is 150 microseconds.

Q*X*SRP - Indicates the normal response to a successfully executed dataway cycle.

/Q*X*SRP - A simple No Q response indicating that the target module was properly addressed but did not execute the desired operation.

/Q*/X*/SRP - Indicates that the TSCC did not allow the desired CAMAC dataway cycle to occur. This is most often due to an arbitration conflict.

/Q*/X*SRP - This line indicates that the target module did not return Q and X. A non-existent or non-functional module, or an invalid function code and sub-address are among the causes for this type of response.

ARBCON - This line denotes an arbitration conflict between the two ports of the TSCC or between the active port and the Block Transfer operation. It is derived from the TSCC response status and is further conditioned by the Port A or Port B configuration of the Driver. ARBCON is most often, if not always, accompanied by assertion of /Q*/X*/SRP.

CRLAM - Indicates that at least one module in the addressed crate is asserting LAM.

AIP - This line is the transferred status of the P1 bussed line of the CAMAC dataway. In most Tevatron system crates, this line reflects the state of the Tevatron Beam Permit hardware loop. AIP asserted indicates that the Abort has been fired and that loop is inhibiting beam.

FAGR - Indicates that a previously attempted aggregate command to the target crate failed. The failure is usually due to conflict with the Block Transfer operation which has higher priority within the TSCC.

TERMINATED RESERVE - This line is the logical or of the CRBT and NRBT status bits of the TSCC response. This line is of special significance to Link Drivers configured for Port B operation.

LINK ERROR - This line is asserted when any number of errors have occurred in the serial transaction. It results from: protocol failure of any of the PIOR response frames; failure of echoed Crate Address, NAF, or Write data to compare with transmitted Crate Address, NAF, or Write data. LINK ERROR may also result from the assertion of PAXE/PBXE or non-assertion of the NAFOKPA/NAFOKPB TSCC status bits. The ALD does not assert LINK ERROR for a TIMEOUT. This is an important difference between the ALD and TSCC Link Driver operation.

## 3 LINK DRIVER REGISTER CONTENT

* Register A(0): BLOCK TRANSFER NAF Read/Write

| D15 | D14 | D13 | - | D9 | D8 | - | D5 | D4 | D3 | D2 | - | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| x | N16 | N8 | N4 | N2 | N1 | A8 | A4 | A2 | A1 | x | F4 | F2 | F1 |

* Register A(1): BLOCK TRANSFER WORD COUNT Read/Write

| D15 | - | D0 |
|---|---|---|
| 32,768 | - | 1 |

The TSCC always returns one more word than the programmed value. Consequently, the A(1) register should be loaded with a value that is one less than the desired transferred word count.

* Register A(2): BLOCK TRANSFER MAXIMUM NO Q Read/Write

| D15 - D8 | D7 - D0 |
|---|---|
| x | 128 - 1 |

* Register A(3): ARBITRATION and CRATE ADDRESS Read/Write

| D15 | D14 - D12 | D11 | D10 | D9 | D8 | D7 - D0 | |
|---|---|---|---|---|---|---|---|
| ALP | x | SCRA | SNRA | RCRB | RNRB | CRATE ADDRESS | Port A |
| ALP | x | SCRB | SNRB | 0/1 | 0/1 | CRATE ADDRESS | Port B |

ALP - Assert Link Priority: When asserted, this control line prevents other connected ALDs from sharing the PIOX and PIOR links. For diagnostic purposes only.

SCRA - Sets the Crate Reserve for Port A.

SNRA - Sets the Slot Reserve for Port A.

RCRB - Resets the Crate Reserve of Port B.

RNRB - Resets the Slot Reserve of Port B.

SCRB - Sets the Crate Reserve for Port B.

SNRB - Sets the Slot Reserve for Port B.

CRATE ADDRESS - Up to 256 different CAMAC crates may be addressed by the ALD.

* Register A(4): PROGRAMMED I/O NAF Read/Write

| D15 | D14 | D13 - D9 | D8 - D5 | D4 - D0 |
|---|---|---|---|---|
| x | N16 | N8 N4 N2 N1 | A8 A4 A2 A1 | F16 F8 F4 F2 F1 |

* Register A(5): WRITE DATA (W16 - W1) Read/Write

| D15 - D0 |
|---|
| W16 - W1 |

* Register A(6): WRITE DATA (W24 - W17) Read/Write

| D15 - D8 | D7 - D0 |
|---|---|
| x | W24 - W17 |

* Register A(7): TRIGGER SERIAL TRANSMISSION Write

| D15 - D0 |
|---|
| x |

* Register A(8): LINK DRIVER STATUS Read

| D15 | D14 | D13 | D12 | D11 | D10 | D9 |
|---|---|---|---|---|---|---|
| BUSY | Q*X*SRP | /Q*X*SRP | /Q*/X*/SRP | ARBCON | /Q*/X*SRP | TIMEOUT |

| D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| LINK ERROR | RF1CK | RF2CK | RF3CK | CACK | NAFCK | EDCK | PADRV | CRLAM |

RF1CK - This line indicates that the first PIOR response frame passed protocol and parity checks.

RF2CK - This line indicates that the second PIOR response frame passed protocol and parity checks.

RF3CK - This line indicates that the third PIOR response frame, if received, passed protocol and parity checks. If a third frame was not expected and not received, RF3CK is forced true.

CACK - This line indicates that the echoed crate address was equal to the transmitted crate address.

NAFCK - This line indicates that the echoed NAF was equal to that which was transmitted.

EDCK - This line indicates that the echoed write data were equal to that which were transmitted. If write data were not transmitted, EDCK is forced true.

PADRV - Assertion of this line indicates that the ALD is configured as a Port A link driver.

* Register A(9): RESPONSE DATA (R16 - R1) Read

| D15 | - | D0 |
|---|---|---|
| R16 | READ DATA | R1 |
| W16 | ECHO WRITE DATA | W1 |
| L16 | LAM DATA | L1 |

* Register A(A): RESPONSE DATA (R24 - R17) Read

| D15 - D8 | D7 - | D0 |
|---|---|---|
| 0 | R24 READ DATA | R17 |
| 0 | W24 ECHO WRITE DATA | W17 |
| 0 | L24 LAM DATA | L17 |

* Register A(B): TSCC RESPONSE STATUS Read

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 |
|---|---|---|---|---|---|---|---|---|---|---|
| Q | X | I | BP | CRLAM | CRA | NRA | CRB | NRB | CRBT | NRBT |

| D4 | D3 | D2 | D1 | D0 | |
|---|---|---|---|---|---|
| BTA | PAN=PBN | PAXE | NAFOKPA | SR2P | Port A |
| BTA | PAN=PBN | PBXE | NAFOKPB | SR4P | Port B |

Q - Indicates that the target module returned Q during the crate dataway cycle.

X - Indicates that the target module returned X during the crate dataway cycle.

I - Indicates that the Inhibit line of the crate dataway is asserted.

BP - Indicates the state of the P1 bussed line of the dataway. Generally "Beam Permit" for Tevatron system crates. BP is the complement of AIP.

CRA - Indicates that Port A has the crate reserved.

NRA - Indicates that Port A has a slot reserved.

CRB - Indicates that Port B has the crate reserved.

NRB - Indicates that Port B has a slot reserved.

CRBT - Indicates that CRB was terminated by Port A. This line is normally asserted by a TSCC clear. It is reset by Port B communications.

NRBT - Indicates that NRB was terminated by Port A. This line is normally asserted by a TSCC clear. It is reset by Port B communications.

BTA - Indicates that the Block Transfer function of the TSCC is active.

PAN=PBN - Indicates that the slot currently addressed is the same as last addressed by the other port.

PAXE - Indicates a detected protocol error for the second or subsequent frame(s) of a Port A PIOX transmission.

PBXE - Similar to PAXE, but for Port B PIOX transmissions.

NAFOKPA - Indicates that the second Port A PIOX frame was properly received with 1's separating the NAF fields and a N that ranged from 0 to 24.

NAFOKPB - Similar to NAKOKPA, but for Port B.

SR2P - Indicates that the Port A PIOX request was allowed and, generally, that a dataway cycle was executed.

SR4P - Indicates that the Port B PIOX request was allowed and, generally, that a dataway cycle was executed.

* Register A(C): TSCC RESPONSE STATUS & ECHO CRATE ADDRESS

Read

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | |
|---|---|---|---|---|---|---|---|---|
| PARDF | PALDF | PAN=BTNA | NAFOKBT | N(24)Q | FAGR | C | Z | Port A |
| PBRDF | PBLDF | PBN=BTNA | BTN16 | BTN8 | BTN4 | BTN2 | BTN1 | Port B |

| D7 | - | D0 |
|---|---|---|
| ECHO CRATE ADDRESS | | |

PARDF - This is the Read Data Flag for Port A. It indicates that there will be a third PIOR response frame containing read data or echoed write data.

PBRDF - Similar to PARDF, but for Port B.

PALDF - This is the LAM Data Flag for Port A. It indicates that there will be a third PIOR response frame containing the status of individual LAMs from slots 1 thru 24. L22 and L23 are always false. L24 is asserted only by FAGR.

PBLDF - Similar to PALDF, but for Port B.

PAN=BTNA - Indicates that the slot addressed by Port A was the same slot being addressed by an active Block Transfer function.

PBN=BTNA - Similar to PAN=BTNA, but for Port B.

NAKOKBT - Indicates a properly received Block Transfer NAF frame. Receipt of N that ranged from 0 to 23, of F that ranged from 0 to 7, and 0's separating the NAF fields is implied.

N(24)Q - Indicated that the desired TSCC N(24) operation was executed.

FAGR - Indicates that the previously attempted aggregate command failed. This line is normally cleared by a Port A read of LAM status.

C - This indicates the state of the dataway Clear line. It is expected to be asserted only during a Port A induced C_*S2 cycle.

Z - This indicates the state of the dataway Initialize line. It is expected to be asserted only during a Port A induced Z_*S2 cycle.

BTN16 thru BTN1 - These lines indicate the slot addressed by an active Block Transfer function and are returned only from Port B. These lines are cleared to zero when the Block Transfer function is off.

* Register A(D): ECHO NAF Read

| D15 | D14 | D13 | - | D9 | D8 | - | D5 | D4 | - | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| x | N16 | N8 | N4 | N2 | N1 | A8 | A4 | A2 | A1 | F16 | F8 | F4 | F2 | F1 |

## 4 LINK DRIVER OPERATION

The ALD is normally Initialized at the beginning of any operation by assertion of the INIT line. This clears the response status of the previous transmission but does not alter the content of the A(0) thru A(6) registers. These registers are then overwritten as necessary and a Trigger Transmission command is generated. The arbitration process commences with the assertion of BUSY. The arbitration algorithm delays the transmission of PIOX frames by at least one microsecond. This delay can be longer, up to 150 microseconds worst case, if the ALD senses that other connected ALDs are actively making use of the PIOX/PIOR links.

The ALD examines the contents of the A(4) register for two specific types of codes. The first is a N(0-23)*A(x)*F(16-23) code which indicates a dataway write operation. This code will cause the transmission of a third PIOX frame consisting of the write data contained in the A(5) and A(6) registers. The second code is N(24)*A(15)*F(16). This is the Block Transfer set-up code to the TSCC and causes the transmission of a third and fourth PIOX frame which consist of A(0), A(1), and A(2) data.

## 5 PHYSICAL LINK ARBITRATION

## 6 CONNECTOR ASSIGNMENTS

## 7 DOCUMENTATION

12345678901234567890123456789012345678901234567890123456789012345678901234567890