VME Quad Ramp Controller
(V473)

Dan McArthur
March 24, 2011

General Description

The V473 is a programmable ramp controller capable of generating four semi-independent, time-based analog outputs. These outputs are updated at a 100 kHz rate.

The V473 also contains digital control capabilities to turn on, turn off, and reset four power supplies. It can also return eight status bits, a ramp enable bit, and a power supply enable bit from each of the regulator supplies.

Features

Output Functions

The ramp outputs will have the form:

output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The output functions of all four channels share a common trigger. Each channel has an independent delay, programmable from 0 to 65535 μsec, between the TCLK trigger event and the start of the output functions.

Note: Although the shortest programmable delay is 0 μsec, at least 10 μsec must be allowed for the FPGA to start the ramp. The V473 will enforce a 10 μsec minimum delay.

Scale Factors

Scale factors are 16 bits long. The upper byte is interpreted as the whole number part and the lower byte is interpreted as the fractional part of the scale factor. Positive and negative scale factors are allowed. The largest negative scale factor is -128.000. The largest positive scale factor is approximately 127.996.

A separate scale factor is programmed for each interrupt level for each channel.

Changes to active scale factors are updated at the start of the next ramp.

Offsets

Offsets are 16 bits long. Positive and negative offsets are allowed. The largest negative offset is -32768. The largest positive offset is 32767.

A separate offset is programmed for each interrupt level for each channel.

Changes to active offsets are updated at the start of the next ramp.

Overflow Errors

The FPGA checks for overflow errors following each calculation and maintains the previously calculated value if an overflow is detected.

Sine Wave Mode (Amplitude Modulation)

The V473 can be configured to play a sine wave with ramping amplitude. The piecewise linear curve defined by f(t), scale factor, and offset becomes the amplitude of the sine wave. Additionally, a programmable frequency and phase are applied to the sine wave.

output = (scale_factor * f(t) + offset) * sin(2πfreq * t + phase)

Frequency is programmable from 0 Hz (0x0000) to 50 kHz (0x8000). Because the DAC output is updated at 100 kHz, larger values (0x8000 to 0xFFFF) will progressively fold back from 50 kHz to 0 Hz due to aliasing. In practice, the output frequency is limited by the slew rate of the output opamp to a few kHz, depending on the desired maximum amplitude of the sine wave.

Phase is programmable from -180° (0x8000 signed) to 179.99° (0x7FFF). When a ramp starts, the sine wave will discontinuously jump to the starting phase.

At the end of a ramp, the sine wave can be configured to free-run at the final amplitude or hold the last value sent to the DAC at a DC level.

Frequency and phase are programmed in the same way as scale factors and offsets. Tables of frequencies and phases are defined for each channel, and entries from these tables are mapped to interrupt levels.

Sweep Mode (Amplitude and Frequency Modulation)

The V473 can also be programmed to play a sine wave with a frequency sweep. This is done by ramping the sine wave's frequency as well as amplitude. The frequency ramp is generated by the next channel's ramp generator. For instance, to play a frequency sweep on Channel 0, we define a ramp (f(t), sf, and offset) on Channel 1 to vary the frequency.

Ch0 output = (scale_factor0 * f0(t) + offset0) * sin(2π[scale_factor1 * f1(t) + offset1] * t + phase0)

At the end of Channel 0's ramp, the sine wave can be configured to free-run at the final amplitude or hold the last value sent to the DAC at a DC level. If configured to free run, at the end of Channel 1's ramp, the sine wave will free run at the final frequency.

Any Channel N can be used to sweep the frequency of any Channel N-1. Channel 0 will sweep the frequency of Channel 3. The channel being used to sweep frequency will still put out a voltage waveform.

Ramp Output

The outputs are provided in analog format (16 bits, +/- 10.000V).

Bias Input

An analog input is supplied that will accept a +/- 5V input. The voltage is not monitored or processed by the V473's FPGA or firmware. This signal will be doubled and analog-added to each channel's ramp output.

ADC Monitoring

Each channel's final output (after adding the Bias Input) is constantly compared to a voltage feedback signal from that channel's power supply. This is accomplished by applying the final output and feedback input to the inputs of a differential instrumentation amplifier. The output of this amplifier is monitored by the FPGA through an ADC and compared to a programmable error threshold value.

Tables

The overall shape of the output function is defined by f(t). Each f(t) is programmed into a table in the V473 as a piecewise linear curve. Each channel will have seventeen possible tables with a maximum of 64 points each. Fifteen of the tables (1-15) are user-definable. The other (table 0) is defined as the "null" ramp. Each point consists of a ramp value V and a delta-t value. The delta-t value is in increments of 10 µsec (1/100 kHz). The last delta-t value of each table must be zero. At the end of each ramp, the final value will be held.

The null ramp is a flat line at 0. A non-zero offset can still be mapped by the interrupt level calling the null ramp. The scale factor mapped to this interrupt level is irrelevant, since zero times anything is still zero.

Table selection is effected by an interrupt. Thirty-two interrupt levels are available. Each is asserted by the 'or' of up to 8 programmed TCLK events. It is impossible to program one given TCLK event to trigger multiple interrupt levels at the same time. Attempts to program a given TCLK event to trigger a second interrupt level will not be processed and will generate an error. Interrupt levels can also be asserted via a write to Mailbox register 0x4202. The complete list of TCLK events can be found in the TCLK Event Definitions document.

The FPGA constantly monitors the TCLK input. When a TCLK event is detected that is programmed to trigger an interrupt level, the FPGA will start a delay timer. With 10 µsec left in the delay, any ramp that is currently running will be aborted, giving the ramp generators time to reset and load operating parameters. As such, a minimum ramp delay of 10 µsec will be enforced.

Tables are selected via pointers with values of 0 to 15 indicating ramp numbers 0 through 15.

Initialized State

When the V473 is powered up or reset, all scale factors will be set to unity (0x0100) and all offsets, frequencies, and phases will be set to zero. All table pointers will be set to zero, and all table values will be set to zero. The clock event table will be filled with 0xFE, which is defined as the “Null Event”.

Mailbox Memory Map (Summary)

Addr	Description
0x0000 – 0x0FFF	Channel 0 Control and Status
0x1000 – 0x1FFF	Channel 1 Control and Status
0x2000 – 0x2FFF	Channel 2 Control and Status
0x3000 – 0x3FFF	Channel 3 Control and Status
Channel Base + …	
0x000 – 0x7FF	Ramp Tables
0x800 – 0x81F	Ramp Map
0x820 – 0x83F	Reserved
0x840 – 0x85F	Scale Factor Map
0x860 – 0x87F	Scale Factors
0x880 – 0x89F	Offset Map
0x8A0 – 0x8BF	Offsets
0x8C0 – 0x8DF	Reserved
0x8E0 – 0x8FF	Delays
0x900 – 0x91F	Frequency Map
0x920 – 0x93F	Frequencies
0x940 – 0x95F	Phase Map
0x960 – 0x97F	Phases
0xA00	Enable/Disable Waveform
0xA01	Sine Wave Mode
0xA02	Power Supply On/Off
0xA03	Power Supply Reset
0xA04	DAC Read/Write
0xA05	Increment/Decrement DAC
0xA06	F(t) Frequency Setting
0xA10	Power Supply Tracking Tolerance
0xA11	Read ADC
0xA20	Power supply status
0xA21	Power Supply Status Nominal
0xA22	Power Supply Status Mask
0xA23	Power Supply Status Error
0xA30	Active Ramp Table
0xA31	Active Scale Factor
0xA32	Active Offset
0xA33	Active Ramp Table Segment
0xA34	Time remaining in current ramp segment
0xA35	Active Sine Wave Frequency
0xA36	Active Sine Wave Phase
0xA37	Final Sine Wave Frequency
0xA38	Final Sine Wave Phase
0xA39	Calculation Overflow Count

0x4000 – 0x42FF	Global Control and Status
0x4000 – 0x40FF	TCLK Trigger Map
0x4100 – 0x41FF	TCLK Event Mask and Image
0x4200	Enable/Disable TCLK-Triggered Interrupt Levels
0x4201	Erase TCLK Event Table
0x4202	Manual Interrupt Level Trigger
0x4210	Current Active Interrupt Level
0x4211	Current Interrupt Level TCLK Trigger Source
0x4220 – 0x423F	Interrupt Level Count
0x4400 –	Diagnostic Data
0x4400	Mailbox Command Interrupt Count
0x4401	Most recent Mailbox Command
0x4402	Most recent invalid Mailbox Command
0x4403	TCLK Event Counter
0x4404	1Hz interrupt count
0x4405	TCLK event error count
0x4406	Last invalid TCLK event received
0x4407	TCLK Parity Error Count
0x4408	TCLK Signal Error Count
0x4409	TCLK Interrupt Count
0x447F	Clear All Diagnostic Counters
0x4480	Memory diagnostic read address (LS16)
0x4481	Memory diagnostic read address (MS16)
0x4482	Read a word in memory
0x4483	Read a block of memory
0x4484	VME Data Bus Diagnostic Read
0x4490	TCLK Status
0xFF00 –	System Information
0xFF00	Module ID number
0xFF01	Firmware version number
0xFF02	FPGA version number
VME Addr 0xXX7FFA	Mailbox Pointer
VME Addr 0xXX7FFC	Word Count/Words Processed
VME Addr 0xXX7FFE	Read/Write Request / Status
VME Addr 0xXX8000	VME IRQ Enable/Disable
VME Addr 0xXX8002	VME IRQ Source
VME Addr 0xXX8004	VME IRQ Mask
VME Addr 0xXX8006	VME IRQ Status/ID (Interrupt Vector)
VME Addr 0xXXFFFE	Reset V473 (Write)

Mailbox (Detailed Description)

The Mailbox is located in a dual-port RAM between the VME interface and the V473's local processor. The mailbox mechanism is structured as follows:

VME Address	Mailbox Function (VME Side)
0xXX0000 – 0xXX7FF8	Data Buffer
0xXX7FFA	Starting Pointer
0xXX7FFC	(Write) Write/Read Req Word Count (Read) Words Processed
0xXX7FFE	Bit 0(W) 1 = Write Request 0 = Read Request Bit 1(R) 1 = Transaction Complete

The V473 will use the Starting Pointer to decode what data or command is being accessed. It will then use the data in the Data Buffer to carry out a write operation or command, or it will carry out a read operation by filling the Data Buffer with <Word Count> 16-bit data points.

Note: The Starting Pointer is a reference to the Mailbox memory map. It is not a reference to a VME address or an address offset inside the dual-port. Any Data Buffer contents should always start at VME address 0xXX0000.

Note: Word Count refers to the number of 16-bit words, not bytes.

The user initiates a transaction by writing to the Read/Write Request register.

When the V473 has finished carrying out a read/write operation or command, it will respond to the VME user in two ways:

1. The local processor will set the Transaction Complete bit and set Words Processed to the actual number of 16-bit words processed. If a problem occurred, Words Processed will be set to something other than Word Count.

2. If VME Interrupts have been enabled, the local processor will set the VME Interrupt Request with an appropriate Status/ID to inform the VME user that the operation is complete.

Note: When carrying out a read or write request, the V473 will not cross major functional boundaries. For example, if Starting Pointer and Word Count are set such that the Data Buffer would begin inside an F(t) table and end in a scale factor table, the operation will be terminated at the end of the F(t) table memory map. The actual number of Data Buffer data points processed will be reported in Words Processed.

Ramp Table Data: <Channel Base> + 0x000 – 0x7FF

Ramp Table Data is stored in f(t), delta-t order. The address is decoded as 0RRR_RNNN_NNNB, where:

RRRR = Ramp Number (0 – 15)
NNNNNN = Ramp profile segment number (0 – 63)
B = Voltage data or delta-t data:
0 = Voltage data V(n)
1 = delta-t data $\Delta t(n)$

Ramp Number 0 is the "null" ramp and cannot be modified.

The delta-t of the last segment must be zero. This is the flag that the V473 uses to know where the ramp ends.

Ramp Table Data

Bits	Bit Definitions
15:0	Ramp Profile Data B = 0: -32768 to 32767 = -10V to 10V B = 1: 0 – 65535, 10µs ticks

Ramp Map: <Channel Base> + 0x800 – 0x81F

The address is decoded as 1000_000L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in the Ramp Map determines which ramp table will be used when interrupt level LLLLL is triggered.

Ramp Map

Bits	Bit Definitions
15:4	Reserved
3:0	Ramp Table Number (0-15)

Scale Factor Map: <Channel Base> + 0x840 – 0x85F

The address is decoded as 1000_010L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in the Scale Factor Map determines which entry of the Scale Factor Table will be used when interrupt level LLLLL is triggered.

Scale Factor Map

Bits	Bit Definitions
15:5	Reserved
4:0	Scale factor map (0 - 31)

Scale Factor Table: <Channel Base> + 0x860 – 0x87F

The address is decoded as 1000_011N_NNNN, where:
NNNNN = Scale Factor Table Entry (0 – 31)

The Scale Factor Table holds a list of scale factors, which are selected by the Scale Factor Map. Entry zero is the “null” scale factor and cannot be modified.

Scale Factor

Bits	Bit Definitions
15:0	Scale factor (-32768 to 32767 = -128.0 – 127.9)

Offset Map: <Channel Base> + 0x880 – 0x89F

The address is decoded as 1000_100L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in the Offset Map determines which entry of the Offset Table will be used when interrupt level LLLLL is triggered.

Offset Map

Bits	Bit Definitions
15:5	Reserved
4:0	Offset map (0 - 31)

Offset Table: <Channel Base> + 0x8A0 – 0x8BF

The address is decoded as 1000_101N_NNNN, where:
NNNNN = Offset Table Entry (0 – 31)

The Offset Table holds a list of voltage offsets, which are selected by the Offset Map. Entry zero is the “null” offset and cannot be modified.

Offset (output voltage)

Bits	Bit Definitions
15:0	Offset (-32768 to 32767 = -10V to 10V)

Delay Table: <Channel Base> + 0x8E0 – 0x8FF

The address is decoded as 1000_111L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in entry LLLLL of the Delay Table determines length of the delay that will be used when interrupt level LLLLL is triggered.

Delay Table

Bits	Bit Definitions
15:0	Ramp Delay (0-65535 microseconds)

Frequency Map: <Channel Base> + 0x900 – 0x91F

The address is decoded as 1001_000L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in the Frequency Map determines which entry of the Frequency Table will be used when interrupt level LLLLL is triggered.

Frequency Map

Bits	Bit Definitions
15:5	Reserved
4:0	Frequency map (0 - 31)

Frequency Table: <Channel Base> + 0x920 – 0x93F

The address is decoded as 1001_001N_NNNN, where:
NNNNN = Frequency Table Entry (0 – 31)

The Frequency Table holds a list of frequencies, which are selected by the Frequency Map. Entry zero is the “null” frequency and cannot be modified.

Note: Frequency entries have an effect on the channel output only if Sine Wave Mode is enabled.

Frequency

Bits	Bit Definitions	
15:0	Frequency	(0 to 32767 = 0 Hz to 50 kHz) (32767 to 65535 = 50 kHz to 0 Hz)

Phase Map: <Channel Base> + 0x940 – 0x95F

The address is decoded as 1001_010L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

The data stored in the Phase Map determines which entry of the Phase Table will be used when interrupt level LLLLL is triggered.

Phase Map

Bits	Bit Definitions
15:5	Reserved
4:0	Phase map (0 - 31)

Phase Table: <Channel Base> + 0x960 – 0x97F

The address is decoded as 1001_011N_NNNN, where:
NNNNN = Frequency Table Entry (0 – 31)

The Phase Table holds a list of Phase, which are selected by the Phase Map. Entry zero is the "null" phase and cannot be modified.

Note: Phase entries have an effect on the channel output only if Sine Wave Mode is enabled.

Phase

Bits	Bit Definitions
15:0	Phase (-32768 to 32767 = -180 to 180 deg)

Enable/Disable Channel Waveform: <Channel Base> + 0xA00

When enabling this channel, the next TCLK trigger will result in normal waveform output for this channel.

When disabling this channel, the next TCLK trigger will result in no waveform output for this channel. The last value written to the DAC will be held. Manual DAC writes will still have effect.

Channel Waveform Enable/Disable

Bits	Bit Definitions
15:1	Reserved
0	1 = Enable 0 = Disable

Sine Wave Mode: <Channel Base> + 0xA01

Sine Wave Mode

Bits	Bit Definitions
15:3	Reserved
2	Free Run Mode (Valid only if Sine Wave Mode = 1) 1 = Sine wave will free-run at the end of a ramp 0 = Output will hold the last value at DC at the end of a ramp
1	Sweep Mode (Valid only if Sine Wave Mode = 1) 1 = Channel N will play a sine wave with frequency determined by Channel N+1's ramp 0 = Channel N will play a sine wave with frequency from the frequency table
0	Sine Wave Mode 1 = Channel will play a sine wave with amplitude defined by f(t) 0 = Channel will play a piecewise linear curve defined by f(t)

Turn Power Supply On/Off: <Channel Base> + 0xA02

Power Supply On/Off

Bits	Bit Definitions
15:1	Reserved
0	1 = Turn On 0 = Turn Off

Reset Power Supply: <Channel Base> + 0xA03

Writing a 1 to this register will reset the power supply for is channel. At the next 1 Hz timer interrupt, the power supply's reset signal will be activated for one second.

Power Supply Reset

Bits	Bit Definitions
15:1	Reserved
0	1 = Reset

DAC Read/Write: <Channel Base> + 0xA04

Writing to this register will **abort any ramp currently playing** and set the DAC output to the requested setting. Reading this register will return the most recent value sent to the DAC.

Write to DAC

Bits	Bit Definitions
15:0	DAC setting (-32768 to +32767 = -10V to 10V)

Increment/Decrement the DAC: <Channel Base> + 0xA05

Writing to this register will set the DAC output to the next higher or lower setting. Writing to this register will **abort any ramp currently playing** and set the DAC output to the requested setting.

Increment/Decrement DAC

Bits	Bit Definitions
15:1	Reserved
0	1 = Increment DAC 0 = Decrement

F(t) Frequency Setting: <Channel Base> + 0xA06

This setting determines the rate at which F(t) will update the DAC.

F(t) Frequency

Bits	Bit Definitions
15:0	Sample Rate Setting 0 = 1 kHz 1 = 5 kHz 2 = 10 kHz 3 = 50 kHz 4 = 100 kHz (reset default)

Power Supply Tracking Tolerance: <Channel Base> + 0xA10

The voltage difference between channel output (after analog summer) and power supply feedback is constantly monitored. If the magnitude (absolute value) of the error exceeds the tolerance for 16 consecutive samples, a power supply tracking error is declared.

Power Supply Tracking Tolerance

Bits	Bit Definitions
15:0	Tolerance (0 to +32767 = 0 to 10V)

Read ADC: <Channel Base> + 0xA11

This reading is the voltage difference between the card output (after analog summer) and the power supply feedback signal.

ADC Data (Read Only)

Bits	Bit Definitions
15:0	ADC reading (-32768 to +32767 = -10V to 10V)

Power Supply Status: <Channel Base> + 0xA20

Power Supply Status

Bits	Bit Definitions
15	Sine Wave Mode Enabled
14	Power Supply Tracking Error
13	Power Supply Reset (1 = Reset output active)
12	Ramp Active
11	Reserved
10	Power Supply Enabled
9	Overflow
8	Ramp Enabled
7:0	State of power supply status inputs (1 = Input Active)

Power Supply Status Nominal: <Channel Base> + 0xA21

The Power Supply Status Nominal value is the value "expected" to be returned by a read of power supply status if no error conditions exist.

Power Supply Status Nominal

Bits	Bit Definitions
15	Sine Wave Mode Enabled
14	Power Supply Tracking Error
13	Power Supply Reset (1 = Reset output active)
12	Ramp Active
11	Reserved
10	Power Supply Enabled
9	Overflow
8	Ramp Enabled
7:0	State of power supply status inputs (1 = Input Active)

Power Supply Status Mask: <Channel Base> + 0xA22

A bit cleared in the Power Supply Status Mask will suppress errors when the actual power supply status bit does not match the nominal status bit.

Power Supply Status Mask

Bits	Bit Definitions
15	Sine Wave Mode Enabled
14	Power Supply Tracking Error
13	Power Supply Reset
12	Ramp Active
11	Reserved
10	Power Supply Enabled
9	Overflow
8	Ramp Enabled
7:0	State of power supply status inputs

Power Supply Status Error: <Channel Base> + 0xA23

A bit set in the Power Supply Status Error register indicates the value of that bit in the power supply status register (0xA20) did not match that bit in the power supply status nominal register (0xA21), and that bit was not cleared in the power supply status mask register (0xA22). Mismatches are latched into the error register.

Writing a 1 to a particular bit will acknowledge that error condition. Once acknowledged, that bit will be read as 0 in subsequent reads and the associated error condition will not cause another VME IRQ until the actual condition has been cleared and reasserted.

Care should be taken when using the acknowledge function. Writing this register sets a flag for the error bit to be cleared at the next 100 Hz interrupt. Writing this register multiple times without first verifying that the flag has been processed by the 100 Hz interrupt (by reading this register again) could result in unexpected operation.

Power Supply Status Error

Bits	Bit Definitions
15	Sine Wave Mode Enabled
14	Power Supply Tracking Error
13	Power Supply Reset
12	Ramp Active
11	Reserved
10	Power Supply Enabled
9	Overflow
8	Ramp Enabled
7:0	State of power supply status inputs

Active Ramp Table: <Channel Base> + 0xA30

Returns which Ramp Table is currently playing.

Active Ramp Table

Bits	Bit Definitions
15:4	Reserved
3:0	Active Ramp Table (0 – 15)

Active Scale Factor: <Channel Base> + 0xA31

The actual value of the Scale Factor in use by the active ramp is returned.

Active Scale Factor (Read Only)

Bits	Bit Definitions
15:0	Active scale factor

Active Offset: <Channel Base> + 0xA32

The actual value of the Offset in use by the active ramp is returned.

Active Offset (Read Only)

Bits	Bit Definitions
15:0	Active offset

Active Ramp Table Segment: <Channel Base> + 0xA33

Active Ramp Table Segment

Bits	Bit Definitions
15:6	Reserved
5:0	Active segment of active ramp table (0 – 63)

Time Remaining in Active Ramp Segment: <Channel Base> + 0xA34

The number of samples remaining in the active ramp segment is returned.

Time Remaining (Read Only)

Bits	Bit Definitions
15:0	Sample Count Remaining

Active Frequency: <Channel Base> + 0xA35

The actual value of the Frequency in use by the active ramp is returned.

Note: This frequency is valid only if Sweep Mode is turned off. This frequency is taken from the frequency table, not the real-time frequency of the sine wave.

Active Frequency (Read Only)

Bits	Bit Definitions
15:0	Active frequency

Active Phase: <Channel Base> + 0xA36

The actual value of the Phase in use by the active ramp is returned.

Note: The phase returned is the starting phase used at the beginning of the ramp, taken from the phase table, not the real-time phase of the sine wave.

Active Phase (Read Only)

Bits	Bit Definitions
15:0	Active phase

Final Frequency: <Channel Base> + 0xA37

The value of the sine wave frequency at the end of the last ramp will be returned. This information is useful when tuning a ramp to end with the sine wave at a particular phase.

Note: This frequency data represents the step size used to reach the final phase in the sine wave look-up table.

Final Frequency (Read Only)

Bits	Bit Definitions
15:0	Final Frequency

Final Phase: <Channel Base> + 0xA38

The value of the sine wave phase at the end of the last ramp will be returned. This information is useful when tuning a ramp to end with the sine wave at a particular phase.

Final Phase (Read Only)

Bits	Bit Definitions
15:0	Final Phase

Calculation Overflow Count: <Channel Base> + 0xA39

The number of calculation overflow errors detected will be returned. Note that because the outputs are updated at a 100kHz rate, this register can count up at a rather high rate. Any write to this register will reset the counter.

Calculation Overflow Count (Write to reset)

Bits	Bit Definitions
15:0	Calculation overflow count

TCLK Trigger Map: 0x4000 – 0x40FF

The address is decoded as 0100_0000_LLLL_LNNN, where:
LLLLL = Interrupt Level (0 – 31)
NNN = TCLK Event Slot (0 – 7)

Up to 8 TCLK events can be programmed to trigger a given Interrupt Level.

TCLK event $FE is defined as the "Null Event". Writing 0xFE to a TCLK Event Slot occupied by another event will erase that event from the TCLK Trigger Map.

A given TCLK event can only be programmed to trigger (at most) one Interrupt Level. Attempts to program a given TCLK event to trigger more than one Interrupt Level will not be processed.

TCLK Trigger Map

Bits	Bit Definitions
15:8	Reserved
7:0	TCLK Event

TCLK Event Mask and Image: 0x4100 – 0x41FF

The address is decoded as 0100_0001_TTTT_TTTT, where:
TTTTTTTT = TCLK Event

The Mask state of a given TCLK Event is returned, along with the Interrupt Level that the TCLK Event would trigger (if Mask State is Active).

TCLK Trigger Map (Read Only)

Bits	Bit Definitions
15:8	Reserved
7	TCLK Event Mask State 1 = Active (Event is used to trigger an Interrupt Level) 0 = Inactive (Event is unused)
6:5	Reserved
4:0	Interrupt Level (Valid only if Mask State is Active)

Enable/Disable TCLK-Triggered Interrupt Levels: 0x4200

When TCLK-Triggered Interrupt Levels are disabled, no TCLK Event will trigger an Interrupt Level. Interrupt levels can still be triggered manually (0x4202). The TCLK Trigger Map remains intact, but will have no effect. When TCLK Events are once again enabled, Interrupt Levels are triggered as defined by the TCLK Trigger Map.

Enable/Disable TCLK-Triggered Interrupt Levels

Bits	Bit Definitions
15:1	Reserved
0	1 = Enable 0 = Disable

Erase TCLK Trigger Map: 0x4201

Writing a 1 to this register will cause the entire TCLK Trigger Map to be erased. This can take a second or so.

Clear TCLK Trigger Map

Bits	Bit Definitions
15:1	Reserved
0	1 = Erase TCLK Trigger Map

Manual Interrupt Level Trigger: 0x4202

Manually trigger an interrupt level. Writing to this register will trigger an Interrupt Level, just as if a TCLK event occurred that was mapped to that Interrupt Level, including delay. If a ramp is active at the time this command is sent, the active ramp will be aborted, just as if a mapped TCLK event had come along while a ramp was active.

Manual Trigger

Bits	Bit Definitions
15:5	Reserved
4:0	Interrupt Level

Active Interrupt Level: 0x4210

The currently (or most recently) active Interrupt Level will be returned.

Active Interrupt Level

Bits	Bit Definitions
15:5	Reserved
4:0	Active Interrupt Level (0 – 31)

Interrupt Level TCLK Trigger Source

Returns which TCLK event triggered the current (or most recent) interrupt level. If $FE is returned, the interrupt level was triggered manually, or no interrupt levels have been triggered since reset.

Interrupt Level TCLK Trigger Source

Bits	Bit Definitions
15:8	Reserved
7:0	Interrupt Level TCLK Trigger Source

Interrupt Level Count: 0x4220 – 0x423F

The address is decoded as 0100_0010_000L_LLLL, where:
LLLLL = Interrupt Level (0 – 31)

A read returns the number of times a particular Interrupt Level has been triggered.

A write will reset the counter for that particular Interrupt Level.

Interrupt Level Count

Bits	Bit Definitions
15:0	Interrupt Level Count

Mailbox Command Interrupt Count: 0x4400

A counter in the V473 increments once every time the Mailbox service routine is entered. The number of Mailbox command interrupts is returned. Any write to this register will reset the counter.

Mailbox Command Interrupt Count (Write to reset)

Bits	Bit Definitions
15:0	Mailbox Command Interrupt Count

Most Recent Mailbox Command: 0x4401

The address of the most recent Mailbox command is returned. Any write to this register will reset it to -1.

Most Recent Mailbox Command

Bits	Bit Definitions
15:0	Address of most recent Mailbox command

Most Recent Invalid Mailbox Command: 0x4402

The address of the most recent invalid Mailbox command is returned. The address of any command that results in an error will be reported here. Any write to this register will reset it to -1.

Most Recent Invalid Mailbox Command

Bits	Bit Definitions
15:0	Address of most recent invalid Mailbox command

Raw TCLK Event Count: 0x4403

Returns the number of raw TCLK events have been detected since reset. Any write to this register will reset the counter.

Raw TCLK Event Count (Write to reset)

Bits	Bit Definitions
15:0	Raw TCLK Event Count

1 Hz Interrupt Count: 0x4404

A counter in the V473 increments once per second. The number of 1Hz interrupts is returned. Any write to this register will reset the counter.

F(3)A(14)

Bits	Bit Definitions
15:0	1 Hz Interrupt Count

TCLK Error Count: 0x4405

This counter is incremented each time an interrupt level is erroneously triggered by an invalid TCLK event. Any write to this register will reset the counter.

TCLK Error Count

Bits	Bit Definitions
15:0	TCLK Error Count

Most Recent Invalid TCLK Event: 0x4406

The last TCLK event that erroneously triggered an interrupt level will be returned. Any write to this register will reset it to -1.

Most Recent Invalid TCLK Event

Bits	Bit Definitions
15:8	Reserved
7:0	Most recent Invalid TCLK Event

TCLK Parity Error Count: 0x4407

This counter is incremented each time a TCLK parity error is detected. Any write to this register will reset the counter.

TCLK Parity Error Count

Bits	Bit Definitions
15:0	TCLK Parity Error Count

TCLK Signal Error Count: 0x4408

This counter is incremented each time a TCLK signal error is detected. Any write to this register will reset the counter.

TCLK Signal Error Count

Bits	Bit Definitions
15:0	TCLK Signal Error Count

TCLK Interrupt Count: 0x4409

This counter is incremented each time the ramp launch interrupt service routine is called. This is usually in response to a mapped TCLK event, but may also be in response to a manual trigger. Any write to this register will reset the counter.

TCLK Interrupt Count

Bits	Bit Definitions
15:0	TCLK Signal Error Count

Clear Diagnostic Counters: 0x447F

Writing a 1 to this register will reset all diagnostic counters to 0x0000.

Clear Diagnostic Counters

Bits	Bit Definitions
15:1	Reserved
0	1 = Clear Diagnostic Counters

Diagnostic Memory Pointer (Least Significant 16 Bits): 0x4480
The user will write the lower (least significant) 16 bits of the Diagnostic Memory Pointer here.

Diagnostic Pointer (15:0)

Bits	Bit Definitions
15:0	Diagnostic Memory Pointer (15:0)

Diagnostic Memory Pointer (Most Significant 16 Bits): 0x4481
The user will write the upper (most significant) 16 bits of the Diagnostic Memory Pointer here.

Diagnostic Pointer (31:16)

Bits	Bit Definitions
15:0	Diagnostic Memory Pointer (31:16)

Read a word in memory: 0x4482

Return a word in memory from an address defined by writing to 0x4480 and 0x4481. Consecutive reads from 0x4482 will return data from the same address.

Memory Word (Single)

Bits	Bit Definitions
15:0	Memory Data

Read a block of memory: 0x4483

Return a word in memory from an address defined by writing to 0x4480 and 0x4481. The address is auto-incremented with each successive read from 0x4483.

Memory Word (Block)

Bits	Bit Definitions
15:0	Memory Data

VME Data Bus Diagnostics: 0x4484

Data written to the VME Data Bus Diagnostics Register will be echoed in the next read from the register. Subsequent reads from the VME Data Bus Diagnostics Register will return data in a continuous loop:

<Written Data>
0x0000
0xFFFF
0x00FF
0xFF00
0x0F0F
0xF0F0
0x3333
0xCCCC
0x5555
0xAAAA
<Written Data>

When writing to this register, the only valid write buffer length is 1. When reading from this register, any read buffer length can be used. The V473 will fill the read buffer with <read_buffer_length> words of the repeating data pattern described above.

VME Data Bus Diagnostics

Bits	Bit Definitions
15:0	VME Data Bus Diagnostic Register

TCLK Status: 0x4490

The TCLK Status register will be returned. The error bits are periodically cleared by the processor.

TCLK Status

Bits	Bit Definitions
15:4	Reserved
3	TCLK Rate (1 = 10 MHz, 0 = 9 MHz)
2	TCLK Signal Error (1 = signal error detected)
1	TCLK Parity Error (1 = parity error detected)
0	TCLK Detect (1 = TCLK carrier detected)

Module ID number: 0xFF00

Module ID

Bits	Bit Definitions
15:0	0x01D9 (473)

Firmware Version Number: 0xFF01

Firmware Version

Bits	Bit Definitions
15:8	Major Revision

7:0	Minor Revision

FPGA Version Number: 0xFF02

FPGA Version

Bits	Bit Definitions
15:8	Major Revision
7:0	Minor Revision

Mailbox Starting Pointer: VME Address 0xXX7FFA

The Mailbox Starting Pointer register tells the V473 which data to put in the mailbox (read) or what to do with data placed in the mailbox (write). The Starting Pointer can be considered analogous to a CAMAC Function/Address code.

Mailbox Command/Address

Bits	Bit Definitions
15:0	Starting Pointer

Mailbox Word Count / Words Processed: VME Address 0xXX7FFC

The Word Count is written by the user to tell the V473 how many data elements to put into, or retrieve from, the mailbox data buffer. This can used to read/write multiple entries of a table with a single transaction.

When the V473 indicates that a transaction has been completed, the user can read Words Processed to find out how many data points were processed. If no error occurred, Words Processed will equal Word Count.

Mailbox Word Count / Words Processed

Bits	Bit Definitions
15:0	(Write) Word Count (Read) Words Processed

Mailbox Read/Write Request / Status: VME Address 0xXX7FFE

The user initiates a transaction by writing to the Read/Write Request register. The user should write to the Mailbox Read/Write Request register only after they have programmed the Starting Pointer, Word Count, and (if a write request) filled the data buffer appropriately. Writing to the Read/Write Request register automatically interrupts the V473's processor, and the V473 will complete the transaction.

When the V473 has completed the transaction, it will set the Transaction Complete bit. The user can poll this bit to check the status of the requested transaction.

Note: When writing to the Read/Write Request register, the user should take care to set the Transaction Complete bit (bit 1) to zero. If set to 1 by the user, status data polled from this register will be meaningless.

Mailbox Read/Write Request / Status

Bits	Bit Definitions
15:2	Unused
1	1 = Transaction Complete (Read Only – should only be written as 0)
0	1 = Write Request 0 = Read Request

VME IRQ Control: VME Address 0xXX8000

Bit 0 enables or disables VME interrupts. The VME User may choose whether or not to receive VME Interrupt Requests from the V473. The VME IRQ is disabled at reset.

Bit 1 selects the mode by which mode the VME IRQ will be cleared. A 0 (default) selects ROAK operation. The VME IRQ will be cleared upon receipt of a VME Acknowledge Cycle. A 1 selects RORA operation. The VME IRQ will be cleared when the VME user writes to the VME Source register.

VME IRQ Control

Bits	Bit Definitions
15:2	Reserved
1	1 = RORA 0 = ROAK
0	1 = Enable VME IRQ 0 = Disable VME IRQ

VME IRQ Source Latched Register: VME Address 0xXX8002

A 1 in a given bit position indicates that the given condition has occurred and has been latched in this register. The condition may or may not still be active. Once latched, the condition will not trigger another VME interrupt until the actual condition has been cleared, the VME user has cleared the bit and the condition is reasserted.

To clear a source bit, write a 1 to that bit. The bit will be cleared, even if the condition is still present. The VME IRQ will not occur again until the actual condition and the source bit have been cleared, then the condition is reasserted.

VME IRQ Source Register

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

VME IRQ Source Mask: VME Address 0xXX8004

A bit cleared in the VME IRQ Mask will suppress assertion of the VME IRQ when the corresponding bit is set in the VME IRQ Source Register.

VME IRQ Source Mask

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

VME IRQ Status/ID Vector: VME Address 0xXX8006
The VME User must program this register with the Status/ID Vector expected to be sent by the V473 during a VME Interrupt Acknowledge cycle.

The V473 is capable of sending a 16-bit Status/ID Vector. The VME user should leave bits 15:8 cleared if the VME processor is only capable of accepting an 8-bit Status/ID Vector.

VME Status/ID Vector

Bits	Bit Definitions
15:0	Status/ID Vector

VME IRQ Source Active Register: VME Address 0xXX8008

A 1 in a given bit position indicates that the given condition is active at this time.

VME IRQ Source Active Register (Read Only)

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

VME IRQ Source Acknowledged Register: VME Address 0xXX800A

A 1 in a given bit position indicates that the given condition is active and has been acknowledged by writing to the VME IRQ Source Latched register. Conditions that are “Active” but not “Acknowledged” will appear in the “Latched” register and may assert the IRQ (depending on the Mask). Conditions that are “Active” and have been “Acknowledged” will not appear in the “Latched” register and will not reassert the IRQ.

VME IRQ Source Acknowledged Register (Read Only)

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

CPLD Version: VME Address 0xXX800C

The version of the VME Interface/FPGA Configuration CPLD will be returned.

CPLD Version (Read Only)

Bits	Bit Definitions
15:8	Major Revision
7:0	Minor Revision

Reset Module: VME Address 0xXXFFFE

Any write to VME Address 0xXXFFFE (Notice: VME Address, not Mailbox Address) will reset the V473. This function is handled by hardware.

Theory of Operation

Ramp Outputs

The V473 user programs the card with the following data:

- Which TCLK events will cause triggers
- Which interrupt levels will activate as a result of TCLK event triggers. Each TCLK event will trigger either zero or one interrupt level, never more than one. Every channel will execute the same interrupt level, but each channel will have its own ramp profile, scale factor, offset, delay, frequency, and phase.
- Delay between TCLK event and start of ramp outputs. Each channel can be programmed with an independent delay.
- A table of ramp profiles (the basic shape of the ramp output). Each channel gets its own table of ramp profiles.
- Which ramp profile to use by each channel for each interrupt level
- A scale factor to use for each interrupt level. Each channel will have a unique scale factor.
- An offset to use for each interrupt level. Each channel will have a unique offset.
- Sine wave frequency and phase. Each channel will have a unique frequency and phase.

The V473 constantly monitors TCLK. Every time a TCLK event is received, the FPGA uses that event as an address to read a RAM containing interrupt level map data. Bit 7 of this data will have been set if this TCLK event is enabled to cause a trigger. Bits 4:0 indicate which interrupt level will be triggered.

If an enabled TCLK event is detected, the FPGA will use the decoded interrupt level as an address to another RAM containing delay data and preset a counter with this data. The counter decrements once every microsecond. When the counter reaches 10 μsec, any active ramp will be aborted and the ramp generator loads from local RAM the appropriate scale factor, offset, frequency, and phase. When the delay counter reaches zero, the FPGA starts sending ramp data to the DAC.

The ramp output will take the following form:
output = scale_factor * f(t) + offset

where:

- scale_factor is a constant scale factor having a range of -128.0 to +127.9
- f(t) is an interpolated function of time which is initiated by a TCLK event. f(t) defines the overall shape of the output function
- offset is a constant offset having a range of -32768 to +32767

The function f(t) is downloaded to the FPGA as a piecewise linear curve. Each point consists of a ramp value V (before being scaled and offset) and a delta-t value. Delta-t_n defines the number of samples (at 10 μsec per sample) between V_n and V_{n+1}.

Samples between points n and n+1 are interpolated as follows:

$$V = scale\_factor * \left(V_{n+1} - \left(\frac{(V_{n+1} - V_n)}{deltat(n)} * samples\_remaining \right) \right) + offset$$

The final delta-t value of f(t) must be zero. A delta-t of zero is the flag the FPGA uses to indicate the end of the ramp. The final V value will be held until the next ramp (or manual set, increment/decrement, etc).

The FPGA constantly monitors ramp calculations for overflows. An overflow will occur if a data point's value would be less than -32768 or greater than 32767. If an overflow is detected, the last valid value is held.

Sine Wave Mode

In sine wave mode, the ramp output calculated above will be used as the amplitude of a sine wave rather than being sent directly to the DAC.

The output will take the following form:
output = (scale_factor * f(t) + offset) * sin(2πfreq + phase)

Sine waves are generated by a look-up table (LUT). The LUT is 4096 steps long. A LUT entry is selected by the upper 12 bits of a 16-bit counter. The counter increments at a 100 kHz rate. The raw data of the frequency setting sets the step size of the counter. The raw data of the phase setting defines the counter's initialization point when a ramp starts.

Each channel has its own LUT. Physically, each LUT exists as a 1024x16-bit RAM in the FPGA. At boot-up, the processor programs the LUT with the first quadrant (first 90 degrees) of a sine wave. This quadrant is used to generate all four quadrants of the sine wave by decoding the top two bits of the LUT pointer.

- Bit 14 = 1: Play quadrant in reverse
- Bit 15 = 1: Invert quadrant value

The wave in the LUT is assumed to be unity amplitude, with signed values. When a ramp value is multiplied by the LUT value, the lower 14 bits of the result are simply dropped.

Because the LUT is a programmable RAM, we are in theory not restricted to playing a sine wave. Any odd wave that could be defined in four symmetrical quadrants could be used (square wave, triangle, etc). For now, the processor is hard-coded to download a sine wave.

Sweep Mode

In sweep mode, the ramp output calculated by channel N will be sent to channel N-1 and used as a frequency.

For example, the output of channel 0 will take the following form:
output = (scale_factor0 * f0(t) + offset0) * sin(2π[scale_factor1 * f1(t) + offset1] + phase)

The ramp output of channel N is still sent to the DAC, generating a waveform that can be used as a reference.

Free-Run Mode

In free-run mode, a sine wave will continue to play at after an amplitude ramp ends. If sweep mode is selected, the amplitude is held constant after the ramp, but the frequency will continue to be modified by channel N+1's ramp until channel N+1's ramp ends. With free-run mode disabled, the last value send to the DAC will be held as a DC value.

ADC Inputs

The output of the V473 (after summer) is compared to an analog feedback signal from the power supply. An error signal is created by applying these two signals to the two sides of a differential instrumentation amplifier. The error signal is read by a sixteen-bit ADC every time the DAC is loaded with new data or every 25.6 μsec (1024 clocks @ 40 MHz), whichever comes first. The digitized error signal is compared to a threshold value, programmed by the user. If the absolute value of the error is greater than the threshold value for sixteen consecutive samples, the power supply is declared "out of tolerance" and an error flag is set.

Processor Memory Map

This section is intended for people who wish to write code to run in the V473. Users of the V473 may also gain greater insight into the V473's sequence of operations.

The V473's software runs on an Altera NiosII processor, embedded in the FPGA. The processor is connected to all of its peripherals automatically by Altera's SOPC Builder tool. SOPC builder automatically assigns base addresses to all of the peripherals. Adding, deleting, or modifying these peripherals usually results in completely different base addresses being assigned. These base addresses are aliased by #define's in the file system.h. System.h is automatically generated by Altera's NiosII IDE. Because the actual base addresses are constantly shifting, the system.h aliases are used in this document instead. The one device that has a locked base address is the flash memory.

1. Flash Memory
Flash memory is hard coded to a base address of 0x00000000. Memory space is reserved for as much as 16 megabytes of flash memory. The V473 board is laid out to accommodate a Spansion (AMD) AM29LV128M or equivalent. A smaller part with equivalent pinout may be substituted.

2. SRAM
Up to two megabytes of SRAM is located at EXT_SSRAM_BASE. The V473 is laid out to accommodate a Cypress CY7C1380 synchronous SRAM or equivalent. A smaller part with equivalent pinout may be substituted.

3. Timers
Three timer peripherals are included. See Chapter 12 of Altera's QuartusII Handbook Volume 5: Embedded Peripherals, "Timer Core With Avalon Interface" for programming information.

The system clock timer (SYS_CLK_TIMER_BASE) is used by the processor to generate system delays, such as when using the usleep() function.

Two other timers are included (TIMER_1SEC_BASE and TIMER_100HZ_BASE) and are intended to be used to generate interrupts at regular 1 second and 10 msec intervals.

4. Ramp Controller (TCLK_RAMP.VHD)

The Ramp Controller is mapped to TCLK_RAMP_0_BASE. It contains the TCLK Decoder, Ramp Launch Control, the Ramp Generators, and the DAC Controller.

4.1. Ramp Launch Control(RAMP_LAUNCH.VHD)

TCLK Trigger Map: Word32 Offset 0x0000 – 0x00FF

The TCLK Trigger Map is stored in a 256x8 SRAM in the FPGA. The Word32 offset is decoded as 0000_0000_TTTT_TTTT, where:

TTTT_TTTT = TCLK Event

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time a TCLK event is received, using the TCLK event as the read address. The FPGA determines whether or not this event is enabled for triggering, and if enabled, the FPGA will load the Active Interrupt Level register and start a delay timer.

TCLK Trigger Map

Bits	Bit Definitions
31:8	Reserved
7	TCLK Event Enable 1 = This TCLK event is enabled to launch the interrupt level in bits 4:0 0 = This TCLK event is disabled
6:5	Reserved
4:0	Interrupt level to be launched by this TCLK event

Ramp Launch Delay: Word32 Offset 0x0100 – 0x017F

The Ramp Launch Delays are stored in four, 32x16 SRAMs in the FPGA. The Word32 offset is decoded as 0000_0001_0CCL_LLLL, where:

CC = Channel Number
LLLLL = Interrupt Level

This SRAM is write-only from the processor.

The FPGA will read this SRAM every time an enabled TCLK event is received, using the triggered interrupt level number as the read address. A delay timer is preset with this data and will decrement once every µsec. When this timer expires, the Ramp Launch Control issues the Ramp Start signal.

Ramp Launch Delay

Bits	Bit Definitions
31:16	Reserved
15:0	Ramp Launch Delay, in µsec

Active Interrupt Level: Word32 Offset 0x0200 (Read)

This register is read-only to the processor.

This register indicates the current active interrupt level.

Active Interrupt Level

Bits	Bit Definitions
31:5	Reserved
4:0	Active Interrupt Level

IRQ Clear: Word32 Offset 0x0200 (Write)

When the processor completes servicing the interrupt from the Ramp Launch module, it should issue a write to this address to clear the interrupt. The simple act of writing to this register clears the interrupt. Data is ignored.

IRQ Clear

Bits	Bit Definitions
31:0	Reserved – Ignored

Manual Interrupt Level Trigger: Word32 Offset 0x0201

Writing to this register will trigger an interrupt level, just as if a TCLK event occurred that was mapped to that interrupt level, including delay. If a ramp is active at the time this command is sent, the active ramp will be aborted, just as if a mapped TCLK event had come along while a ramp was active.

This register is write-only.

Manual Ramp Trigger

Bits	Bit Definitions
31:5	Reserved
4:0	Interrupt Level

Interrupt Level TCLK Source: Word32 Offset 0x0202

This register indicates which TCLK event triggered the current (or most recent) interrupt level. If 0xFE is returned, the interrupt level was triggered manually, or there have been no interrupt levels triggered since reset.

This register is read-only.

Interrupt Level TCLK Source

Bits	Bit Definitions
31:8	Reserved
7:0	Interrupt Level TCLK source

Disable TCLK-Triggered Interrupt Levels: Word32 Offset 0x0203

Use this register to disable TCLK-triggered interrupt levels for all four channels. When this register is set, the TCLK trigger map remains intact, but the state machine that watches for mapped TCLK events is inhibited. Interrupt levels can still be manually triggered.

Disable TCLK-Triggered Interrupt Levels

Bits	Bit Definitions
31:1	Reserved
0	1 = Disable 0 = Enable

Abort Current Ramp: Word32 Offset 0x0204

This register will terminate any currently running ramp. The last value sent to the DAC will be held until the next ramp starts or until the DAC is manually written.

This register is write-only.

Abort Current Ramp

Bits	Bit Definitions
31:4	Reserved
3	Abort Channel 3 Ramp
2	Abort Channel 2 Ramp
1	Abort Channel 1 Ramp
0	Abort Channel 0 Ramp

Ramp Generation (RAMP_CTRL.VHD)

Each channel has its own ramp generator. The memory map is:
Channel 0: TCLK_RAMP_0_BASE + 0x0000
Channel 1: TCLK_RAMP_0_BASE + 0x4000
Channel 2: TCLK_RAMP_0_BASE + 0x8000
Channel 3: TCLK_RAMP_0_BASE + 0xC000

F(t) Table: Word32 Offset 0x0000 – 0x07FF

F(t) data is stored in a 2048x16 SRAM in the FPGA. The Word32 offset is decoded as 0000_0RRR_RNNN_NNNB, where:
RRRR = Ramp Number (0 – 15)
NNNNNN = F(t) table entry number (0 – 63)
B = Voltage data or delta-t data:
0 = Voltage data V(n)
1 = delta-t data $\Delta t(n)$

This SRAM is write-only to the processor.

The Ramp Generator begins reading this SRAM after the Ramp Start signal is received from the Ramp Launch module. The Ramp Generator updates the DAC every 10 μsec until it reads zero for delta-t.

F(t) Table

Bits	Bit Definitions
31:16	Reserved
15:0	Voltage data (-32768 – +32767) = -10 to 10 V Delta-t data (0 – 65535) = 0 to 655350 μsec

Ramp Map: Word32 Offset 0x0800 – 0x081F

Ramp Map data is stored in a 32-word segment of a 256x16 SRAM in the FPGA. The Word32 offset is decoded as 1000_000L_LLLL, where:
LLLLL = Interrupt Level

This SRAM is write-only to the processor.

The Ramp Generator reads this SRAM after the Ramp Abort signal is received from the Ramp Launch module, indicating that a new ramp is pending. The Ramp Map data stored here is used to choose which ramp to play once the Ramp Start signal is received. Ramp number RRRR will be played in response to Interrupt Level LLLLL.

Ramp Map

Bits	Bit Definitions
31:14	Reserved
3:0	Ramp Map (0 – 15)

Scale Factors: Word32 Offset 0x0820 – 0x083F

Scale Factor data is stored in a 32-word segment of a 256x16 SRAM in the FPGA. The Word32 offset is decoded as 1000_001L_LLLL, where:

LLLLL = Interrupt Level

This SRAM is write-only to the processor.

The Ramp Generator reads this SRAM after the Ramp Abort signal is received from the Ramp Launch module, indicating that a new ramp is pending. The Scale Factor data stored here is will be used in response to Interrupt Level LLLLL.

Scale Factor

Bits	Bit Definitions
31:16	Reserved
15:0	Scale Factor (-32768 – +32767 = -128.0 to +127.9)

Offsets: Word32 Offset 0x0840 – 0x085F

Offset data is stored in a 32-word segment of a 256x16 SRAM in the FPGA. The Word32 offset is decoded as 1000_010L_LLLL, where:

LLLLL = Interrupt Level

This SRAM is write-only to the processor.

The Ramp Generator reads this SRAM after the Ramp Abort signal is received from the Ramp Launch module, indicating that a new ramp is pending. The Offset data stored here will be used in response to Interrupt Level LLLLL.

Offset

Bits	Bit Definitions
31:16	Reserved
15:0	Offset (-32768 – +32767 = -10V to +10V)

LUT Step Size (Frequency): Word32 Offset 0x0860 – 0x087F

LUT step size data is stored in a 32-word segment of a 256x16 SRAM in the FPGA. The Word32 offset is decoded as 1000_011L_LLLL, where:

LLLLL = Interrupt Level

This SRAM is write-only to the processor.

The Ramp Generator reads this SRAM after the Ramp Abort signal is received from the Ramp Launch module, indicating that a new ramp is pending. The LUT Step Size data stored here will be used in response to Interrupt Level LLLLL.

LUT Step Size translates directly into wave frequency. 0 – 32767 = 0 Hz – 50 kHz. 32768 – 65535 = 50 kHz – 0 Hz.

LUT Step Size

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Step Size

LUT Phase: Word32 Offset 0x0880 – 0x089F

LUT phase data is stored in a 32-word segment of a 256x16 SRAM in the FPGA. The Word32 offset is decoded as 1000_100L_LLLL, where:

LLLLL = Interrupt Level

This SRAM is write-only to the processor.

The Ramp Generator reads this SRAM after the Ramp Abort signal is received from the Ramp Launch module, indicating that a new ramp is pending. The LUT Phase data stored here will be used in response to Interrupt Level LLLLL.

LUT Phase defines the point to which the LUT pointer counter is initialized when a ramp starts. LUT Phase translates directly into wave phase. 0 – 65535 = 0 – 360 degrees.

LUT Phase

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Phase

DAC Value: Word32 Offset 0x0A00

Reading this register returns the most recent programmed DAC value.

Writing this register while the ramp is active has no effect. Otherwise, writing this register sends data to the DAC.

Note: From the processor's point of view, this data value is read and written as a signed, 16-bit value between -32768 and +32767, representing a desired voltage between -10V and +10V. The actual data sent to the DAC is translated to account for actual hardware requirements. See the DAC Controller section for more information.

Each Ramp Generator sends its own DAC Update signal to the DAC Controller every 10 µsec during an active ramp, or in response to a manual DAC write.

DAC Value

Bits	Bit Definitions
31:16	Reserved
15:0	DAC Value (-32768 – +32767 = -10V to +10V)

Ramp/Power Supply Status: Word32 Offset 0x0A01

This register returns ramp and power supply status. Writes are necessary only to clear the Overflow Status bit.

Ramp/Power Supply Status

Bits	Bit Definitions
31:14	Reserved
13	Power Supply Reset Status 1 = PS reset output active
12	Ramp Active 1 = Ramp is active
11	Power Supply Interlock Status 1 = PS Interlock input is active (Tied Active in FPGA, ignore)
10	Power Supply Enable Status 1 = PS Enable output is active
9	Overflow Status 1 = A mathematical overflow has occurred. Write 0 to this bit to clear.
8	Ramp Enabled 1 = Ramp is enabled. This is a status bit only. Writes will have no effect.
7:0	Reserved

Sample Count Remaining: Word32 Offset 0x0A03

This read-only register returns the number of samples remaining in the current segment of the active F(t) piecewise-linear curve.

Sample Count Remaining

Bits	Bit Definitions
31:12	Reserved
11:0	Samples remaining

Scale Factor in Use: Word32 Offset 0x0A04 (Read Only)

Reading this register returns the actual value of the scale factor in use or most recently used.

Scale Factor in Use

Bits	Bit Definitions
31:16	Reserved
15:0	Scale Factor (-32768 – +32767 = -128.0 to +127.9)

Offset in Use: Word32 Offset 0x0A05

Reading this register returns the actual value of the offset in use or most recently used.

Offset in Use

Bits	Bit Definitions
31:16	Reserved
15:0	Offset (-32768 – +32767 = -10V to +10V)

Power Supply Enable: Word32 Offset 0x0A06

Writing to this register enables or disables the power supply.

This register is write-only. The power supply enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Enable 1 = Enable

Power Supply Reset: Word32 Offset 0x0A07

Writing to this register sets the Power Supply Reset request. The request is serviced during the next 1 Hz timer interrupt.

This register is write-only. The power supply reset state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Power Supply Reset 1 = Request Reset

Ramp Enable: Word32 Offset 0x0A08

Writing to this register enables or disables the ramp controller. Writing during an active ramp will have no immediate effect. The ramp enable bit inhibits the ramp controller's state machine from starting, but has no effect while the state machine is running.

This register is write-only. The ramp enable state is read from the Ramp/Power Supply Status register.

Power Supply Enable

Bits	Bit Definitions
31:1	Reserved
0	Ramp Enable 1 = Enable

Ramp Active Segment: Word32 Offset 0x0A09

This register indicates which segment of an F(t) ramp profile is currently active. This register is read-only.

Ramp Active Segment

Bits	Bit Definitions
31:6	Reserved
5:0	Active Segment

Calculation Overflow Count: Word32 Offset 0x0A0A

This register increments every time a calculation overflow is detected. As calculations happen at a 100kHz rate, this register can wrap up rather quickly.

Any write to this register will clear it to 0x0000.

Calculation Overflow Count

Bits	Bit Definitions
31:16	Reserved
15:0	Calculation Overflow Count

F(t) Sample Period: Word32 Offset 0x0A0B

Writing to this register sets the sample period (and thus, the frequency) of the F(t) refresh rate to the DAC. Writing N to this register sets the period to (N+1) * 100 nsec. For example, writing 99 will set the period to (99+1) * 100 nsec = 10 μsec.

Reading this register returns the value of the F(t) Sample Period register.

F(t) Sample Period

Bits	Bit Definitions
31:16	Reserved
15:0	F(t) sample period

LUT Step Size (Frequency) in Use: Word32 Offset 0x0A20

Reading this register returns the actual value of the LUT Step Size in use or most recently used.

LUT Step Size in use

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Step Size

LUT Phase in use: Word32 Offset 0x0A21

Reading this register returns the actual value of the LUT Phase in use or most recently used.

LUT Phase

Bits	Bit Definitions
31:16	Reserved
15:0	LUT Phase

LUT Mode: Word32 Offset 0x0A22

This register is used to enable and disable LUT Mode (Sine Wave Mode), Sweep Mode, and Free-Run Mode.

LUT Phase

Bits	Bit Definitions
31:3	Reserved
2	1 = Enable Free-Run Mode
1	1 = Enable Sweep Mode
0	1 = Enable LUT Mode (Sine Wave Mode)

Final LUT Step Size: Word32 Offset 0x0A23

This register will return the final LUT step size at the end of a ramp. The value returned is the step size used to reach the final phase at the end of a ramp. This information may be useful when tuning a ramp to end with the sine wave at a particular phase.

This register is read-only.

Final LUT Step Size

Bits	Bit Definitions
31:16	Reserved
15:0	Final LUT Step Size

Final LUT Phase: Word32 Offset 0x0A24

This register will return the final LUT phase at the end of a ramp. This information may be useful when tuning a ramp to end with the sine wave at a particular phase.

This register is read-only.

Final LUT Phase

Bits	Bit Definitions
31:16	Reserved
15:0	Final LUT Phase

Look-Up Table: Word32 Offset 0x0C00 – 0x0FFF

Each channel's LUT data is stored in a 1024x16 SRAM in the FPGA. The Word32 offset is decoded as 0000_11NN_NNNN_NNNN, where:

NNNNNNNNNN = LUT table entry number (0 – 1023)

The Look-Up Tables contain only the first quadrant of a wave. The other three quadrants are reproduced by time-reversal and data inversion.

It is assumed that the data in the LUT is signed and that the amplitude of the wave described is unity (1).

4.2. TCLK Receiver

Information about the TCLK Receiver is located starting at TCLK_RAMP_0_BASE + 0x12000.

TCLK Status: Word32 Offset 0x0000

This register indicates the status of the TCLK signal. A '1' in any bit position can be cleared by writing a '0' to that bit.

TCLK Status

Bits	Bit Definitions
31:3	Reserved
2	1 = TCLK signal error detected
1	1 = TCLK parity error detected
0	1 = TCLK signal is present

Raw TCLK Event Count: Word32 Offset 0x0001

This register indicates how many TCLK events the card has detected since reset. It will count up to 65535, then roll over to 0 and continue counting.

This is a count of raw TCLK events, not a TCLK interrupt level count.

Any write to this register will clear it to 0x0000.

Raw TCLK Event Count

Bits	Bit Definitions
31:16	Reserved
15:0	TCLK Event Count

5. ADC Controller (ADC_CTRL.VHD)
The ADC Controller is mapped to ADC_CTRL_0_BASE. The ADC data is automatically updated every time the DAC is updated or every 25.6 µsec (1024 clocks @ 40MHz), whichever comes first.

ADC0 Data: Word32 Offset 0x0000

Reading this register returns ADC0 data. ADC0 reads the difference between the Channel 0 output (after analog summer) and the power supply 0 feedback input.

ADC0 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC0 Data (-32768 – 32767 = -10V to 10V)

ADC1 Data: Word32 Offset 0x0001

Reading this register returns ADC1 data. ADC1 reads the difference between the Channel 1 output (after analog summer) and the power supply 1 feedback input.

ADC1 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC1 Data (-32768 – 32767 = -10V to 10V)

ADC2 Data: Word32 Offset 0x0002

Reading this register returns ADC2 data. ADC2 reads the difference between the Channel 2 output (after analog summer) and the power supply 2 feedback input.

ADC2 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC2 Data (-32768 – 32767 = -10V to 10V)

ADC3 Data: Word32 Offset 0x0003

Reading this register returns ADC3 data. ADC3 reads the difference between the Channel 3 output (after analog summer) and the power supply 3 feedback input.

ADC3 Data

Bits	Bit Definitions
31:16	Reserved
15:0	ADC3 Data (-32768 – 32767 = -10V to 10V)

Channel 0 Tolerance: Word32 Offset 0x0004

Sets or returns the Channel 0 tolerance.

If the absolute value of the ADC0 reading is greater than the Channel 0 Tolerance for sixteen consecutive samples, Channel 0 is declared “out of tolerance” and the Channel 0 Out Of Tolerance bit will be set.

Channel 0 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 0 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 1 Tolerance: Word32 Offset 0x0005

Sets or returns the Channel 1 tolerance.

If the absolute value of the ADC1 reading is greater than the Channel 1 Tolerance for sixteen consecutive samples, Channel 1 is declared “out of tolerance” and the Channel 1 Out Of Tolerance bit will be set.

Channel 1 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 1 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 2 Tolerance: Word32 Offset 0x0006

Sets or returns the Channel 2 tolerance.

If the absolute value of the ADC2 reading is greater than the Channel 2 Tolerance for sixteen consecutive samples, Channel 2 is declared “out of tolerance” and the Channel 2 Out Of Tolerance bit will be set.

Channel 2 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 2 Tolerance (-32768 – 32767 = -10V to 10V)

Channel 3 Tolerance: Word32 Offset 0x0007

Sets or returns the Channel 3 tolerance.

If the absolute value of the ADC3 reading is greater than the Channel 3 Tolerance for sixteen consecutive samples, Channel 3 is declared “out of tolerance” and the Channel 3 Out Of Tolerance bit will be set.

Channel 3 Tolerance

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 3 Tolerance (-32768 – 32767 = -10V to 10V)

ADC Status: Word32 Offset 0x0008

Reading this register returns the Out Of Tolerance bits for all four channels. Writing 0 to a set bit will clear it.

ADC Status

Bits	Bit Definitions
31:4	Reserved
3	Channel 3 Out Of Tolerance 1 = Out Of Tolerance
2	Channel 2 Out Of Tolerance 1 = Out Of Tolerance
1	Channel 1 Out Of Tolerance 1 = Out Of Tolerance
0	Channel 0 Out Of Tolerance 1 = Out Of Tolerance

6. DAC Controller (DAC_CTRL.vhd)

The DAC Controller for each channel is mapped to TCLK_RAMP_0_BASE + 0x11000 + 0x400*Channel. The DAC Controller takes programmed DAC values from the Ramp Controller. The programmed DAC values are translated before actually going to the DAC to account for three things:

- The DAC output gets inverted by the summing amplifier, so the actual DAC data must be "pre-inverted"
- Because there are an even number of possible DAC codes, after inversion the DAC value is further shifted by one count, to ensure that zero still maps to zero, and not -1.
- The Burr-Brown DAC7744 used on the V473 expects a different data format: 0 to 65535 (unsigned 16 bit) for -10V to +10V, instead of -32768 to +32767 (signed 16 bit).

Anyone watching actual data transactions between the FPGA and the DAC should keep this translation in mind. The translation formula is:

```
Actual DAC Data = not(Programmed DAC Data) + 0x8001
```

Any carry bit resulting from this calculation is dropped.

Exception: Programmed DAC Value 0x8000 maps directly to 0xFFFF. Otherwise, the single case of -10.0000V would come out as 10.0000V.

Translation examples:

Programmed Output Voltage	Programmed DAC Data	Actual DAC Data	DAC Output	Board Output
9.9997V	0x7FFF	0x0001	-9.9997V	9.9997V
0.0000V	0x0000	0x8000	0.0000V	0.0000V
-0.0003V	0xFFFF	0x8001	0.0003V	-0.0003V
-9.9997V	0x8001	0xFFFF	9.9997V	-9.9997V
-10.0000V	0x8000	0xFFFF	9.9997V	-9.9997V

For diagnostic purposes, the actual DAC data is made available, read-only.

Actual DAC Data: Word32 Offset 0x0000

This register returns the actual, post-translation data programmed into the DAC.

Actual DAC Data

Bits	Bit Definitions
31:16	Reserved
15:0	Channel 0 DAC Data (0 – 65535)

7. Front Panel LEDs

The front panel LEDs are mapped to LED_DATA_0_BASE. Writing 0 to any of these bits will turn that LED on. The LED register is write-only.

Front Panel LEDs

Bits	Bit Definitions
31:8	Reserved
7	Heartbeat
6	Ramp 0 Enabled
5	Ramp 1 Enabled
4	Ramp 2 Enabled
3	Ramp 3 Enabled
2	LAM
1	Reserved for MDAT Present
0	TCLK Present

8. IP Module (Power Supply Status)

An interface is provided to a standard IndustryPack (IP) Module. It is intended that the IP slot will be populated with a 32-bit, isolated, digital input card. The 32 inputs would be used for digital power supply status inputs (4 channels x 8 bits). However, the interface is implemented generically enough that other IP modules could be used. Power supply status is mapped to IP_DIGIN_0_BASE.

Power Supply Status

Addr	Bit Definitions
0	Power Supply 0 Status
1	Power Supply 1 Status
2	Power Supply 2 Status
3	Power Supply 3 Status

9. VME Interface
The VME interface is mapped to VME_IF_0_BASE.

VME IRQ Source Active: Word32 offset 0x0000 – 0x0001

The VME IRQ Source Active register is written to indicate the current status of VME IRQ sources. A 1 in a given bit position indicates that the given condition is currently active. A bit written to 1 will be latched in the VME IRQ Source Latched register.

The VME IRQ Source Register can only be read or written 8 bits at a time. A Word32 transaction to offset 0x0000 transmits bits 7:0. A Word32 transaction to 0x0001 transmits bits 15:8.

VME IRQ Source Register

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

VME IRQ Source Latched: Word32 offset 0x0002 – 0x0003

The VME IRQ Source Latched register indicates which bits written to the VME IRQ Source Active register are still latched in the VME interface. The VME bus also has access to this register. The VME user uses this data to determine which condition(s) caused a VME interrupt. The VME user clears this register to acknowledge receipt of the interrupt condition.

The VME IRQ Latched Register can only be read or written 8 bits at a time. A Word32 read from offset 0x0000 reads bits 7:0. A Word32 read from 0x0001 reads bits 15:8

VME IRQ Source Register (Read Only)

Bits	Bit Definitions
15	VME Command Error
14	Calculation Error (Overflow)
13	Unused
12	TCLK Missing
11	Unused
10	Unused
9	Power Supply Tracking Error
8:5	Unused
4	VME Command/Read/Write Complete
3	Power Supply 3 Error
2	Power Supply 2 Error
1	Power Supply 1 Error
0	Power Supply 0 Error

10. Dual-Port Memory Interface
The Dual-Port Memory interface is mapped to DP_IF_0_BASE.

There is a 16k x 16-bit dual-port memory between the VME Interface and the local processor. The dual-port is meant to be used as a mailbox between the VME Bus and the local processor. Each 16-bit word is accessed as the lower 16 bits of a 32-bit word. In other words, a Word32 address offset must be used to access each memory location. Byte-wise access to the dual-port is not supported.

The Dual-Port Memory Interface will interrupt the local processor if the VME Interface writes any data to dual-port address 0x3FFF (VME24 Address 0xXX7FFE). The interrupt is cleared when the local processor reads from dual-port address 0x3FFE.

The mailbox mechanism is structured as follows:

Dual-Port Address	Mailbox Function (VME Side)	Mailbox Function (Local Side)
0x0000 – 0x3FFC	Data Buffer	Data Buffer
0x3FFD	Starting Pointer	Starting Pointer Read will clear local IRQ
0x3FFE	(Write) Word Count (Read) Words Processed	(Read) Word Count (Write) Words Processed Read will clear local IRQ
0x3FFF	Bit 0(W) 1 = Write Req 0 = Read Req Bit 1(R) 1 = Transaction Complete Write will set local IRQ	Bit 0(R) 1 = Write Req 0 = Read Req Bit 1(W) 1 = Transaction Complete

A memory map will be defined for the user on the other end of the VME bus. The user will refer to this memory map to set the Starting Pointer for data and command access. The VME User's memory map will not correspond 1-for-1 with the local processor's memory map. The local processor will use the Starting Pointer to decode what data or command is being accessed. It will then use the data in the Data Buffer to carry out a write operation or command, or it will carry out a read operation by filling the Data Buffer with <Word Count> data points.

Note: The Starting Pointer is a reference to the Mailbox memory map. It is not a reference to an address offset inside the dual-port. Any Data Buffer contents should always start at dual-port address 0x0000.

When the local processor has finished carrying out a read/write operation or command, it will respond to the VME user in two ways:

3. The local processor will set the Transaction Complete bit and set Words Processed to the actual number of 16-bit words processed. If a problem occurred, Words Processed will be set to something other than Word Count.

4. If VME Interrupts have been enabled, the local processor will set the VME Interrupt Request with an appropriate Status/ID to inform the VME user that the operation is complete.

Note: When carrying out a read/write request, the local processor will not cross major functional boundaries. For example, if Starting Pointer and Word Count are set such that the Data Buffer would begin inside an F(t) table and end in a scale factor table, the operation will be terminated at the end of the F(t) table memory map. The actual number of Data Buffer data points processed will be reported in Words Processed.

11. FPGA Version (FPGA_VERSION.VHD)
The FPGA version is contained in a small module dedicated to this purpose only. The module is mapped to FPGA_VERSION_0_BASE.

FPGA Version

Bits	Bit Definitions
15:8	Major Revision
R7:R0	Minor Revision

VME Base Address

The V473 occupies 64k (0x1 0000) of VME A24D16 address space. The base address of the card is set with a DIP switch, SW1. Switch positions 1:8 correspond to VME Address bits 23:16, as shown in Figure 1.

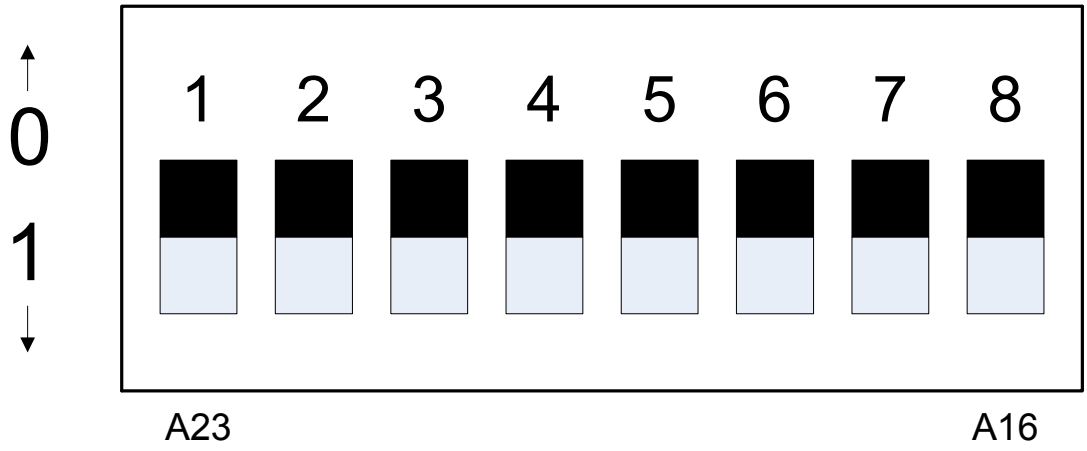

Figure 1: Base Address DIP Switch

VME IRQ Select

The V473 can drive any one of the seven VME IRQ's (IRQ1 – IRQ7). The IRQ is selected by placing a jumper on the one of the jumper headers labeled IR1 – IR7.

Additionally, jumpers must be placed on IS1 – IS3 to select which Interrupt Acknowledge cycle to respond to. IS[3:1] represent a 3-bit field intended to correspond with the IRQ selected. A jumper placed on ISx is a zero. An open ISx is a 1. For example, Figure 2 shows IR[7:1] and IS[3:1] set up for IRQ1.

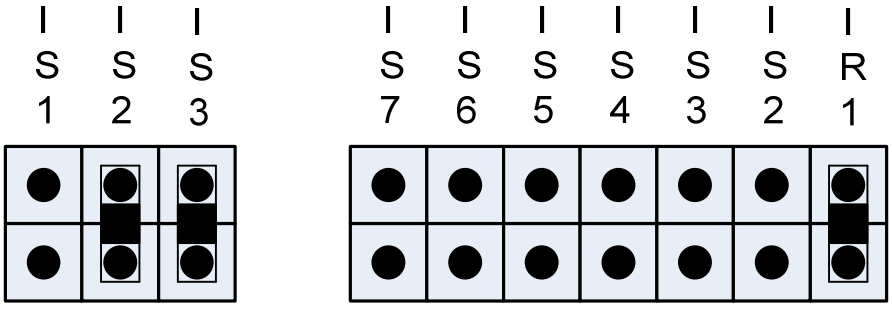

Figure 2: IRQ Selection (IRQ1 Shown)

I/O Connections (P2)

Terminal	Function
A1	Opto Anode Supply - 5 Volts provided by Supply 0
A2	Status Input 0-1 - (pull low for active state)
A3	Status Input 0-2
A4	Status Input 0-3
A5	Status Input 0-4
A6	Status Input 0-5
A7	Status Input 0-6
A8	Status Input 0-7
A9	Status Input 0-8
A10	Opto Anode Supply - 5 Volts provided by Supply 1
A11	Status Input 1-1 - (pull low for active state)
A12	Status Input 1-2
A13	Status Input 1-3
A14	Status Input 1-4
A15	Status Input 1-5
A16	Status Input 1-6
A17	Status Input 1-7
A18	Status Input 1-8
A19	Interlock Input 3 (Ignored)
A20	Interlock Input 1 (Ignored)
A21	TTL Output - Reset Supply 3
A22	TTL Output - Reset Supply 2
A23	TTL Output - Reset Supply 1
A24	TTL Output - Reset Supply 0
A25	Analog Current Readback 3
A26	Analog Current Readback 2
A27	Analog Current Readback 1
A28	Analog Current Readback 0
A29	Analog Reference Ground 3
A30	Analog Reference Ground 2
A31	Analog Reference Ground 1
A32	Analog Reference Ground 0
B2	Digital Gnd
B12	Digital Gnd
B22	Digital Gnd
B31	Digital Gnd
C1	Opto Anode Supply - 5 Volts provided by Supply 2
C2	Status Input 2-1 - (pull low for active state)
C3	Status Input 2-2
C4	Status Input 2-3
C5	Status Input 2-4
C6	Status Input 2-5
C7	Status Input 2-6
C8	Status Input 2-7
C9	Status Input 2-8
C10	Opto Anode Supply - 5 Volts provided by Supply 3
C11	Status Input 3-1 - (pull low for active state)
C12	Status Input 3-2

C13	Status Input 3-3
C14	Status Input 3-4
C15	Status Input 3-5
C16	Status Input 3-6
C17	Status Input 3-7
C18	Status Input 3-8
C19	Interlock Input 2 (Ignored)
C20	Interlock Input 0 (Ignored)
C21	TTL Output - Enable Supply 3
C22	TTL Output - Enable Supply 2
C23	TTL Output - Enable Supply 1
C24	TTL Output - Enable Supply 0
C25	Analog Bias Input 3
C26	Analog Bias Input 2
C27	Analog Bias Input 1
C28	Analog Bias Input 0
C29	Analog Reference Output 3
C30	Analog Reference Output 2
C31	Analog Reference Output 1
C32	Analog Reference Output 0