

CHECKOUT PROCEDURE FOR BOOSTER SSD LLRF CHASSIS

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1. Check all power supply voltages ($\pm 15V$ on Power One Supply, $\pm 12V$ and $\pm 5V$ on the Voltage Regulator Board (0332.00-EB-182291)). These voltages should all be within $\pm 0.2V$ from the nominal voltage.
2. Measure Pin 6 of U6 on the Phase Shifter board (0332-EC-182148) with a DVM. Use the mV scale setting to measure the offset. Adjust R22 on the Phase Shifter board to read 0V on Pin 6 of U6. Adjust R15 on the Variable Gain Amplifier board (9530-EC-182089) to read 0V on Pin 6 of U2.
3. Calibrate a Network Analyzer using a full 2-port calibration. Use phase-stable cables (orange Times Microwave cable, 5 ft in length) to perform the calibration. Set the Network Analyzer power to -19dBm, the number of points to 1601, and the frequency range from 10MHz to 80MHz. Turn on averaging while performing all calibration steps. Use 25 steps with an IF Bandwidth of 10kHz for averaging (E5071C is the preferred Network Analyzer to use). Perform the calibration procedure with the calibration standards on both the input and output cables (Type N standards mated directly to the Type N connectors of the cable). After the standards are measured, perform a thru calibration using a Type N female to BNC male adapter on both cable ends and a BNC bullet (female feedthrough). Check to verify that the calibration is ok.
4. Set up 2 precision voltage sources, one set to +7V, and the other set to 1V. Connect the +7V source to the SSD Program spigot on the rear panel of the chassis. Use a Datel Voltage Calibrator DVC-8500 to set up the 1V source. Don't connect the 1V source to the Phase CTRL spigot on the rear panel just yet.
5. Set up the Network Analyzer to measure S21 (log magnitude), S21 (phase), and S11 (return loss, log magnitude). Place markers at 37MHz, 45MHz, and 53MHz. S21 should measure $\sim 28dB$ ($\pm 0.2dB$ variation is ok over the 37MHz-53MHz bandwidth) through the chassis. Final gain calibration will take place in step 8. This step ensures that the LLRF Chassis is within reasonable specifications. As long as S11 measures less than -18dB of return loss over the 37MHz-53MHz

bandwidth, the input impedance of the LLRF Chassis is ok. Tune the electrical delay such that the phase response is flat ($\pm 2^\circ$) over the 37MHz-53MHz bandwidth. Averaging should be turned off to speed up the phase adjustment process. Typical network analyzer measurements are shown in Figures 2, 3, and 4. Use an E5071C Network Analyzer for doing the measurements.

6. With the Datel DC source set to 1V, connect the output of the source to the Phase CTRL input of the chassis. Check to make sure that the phase shifts between $\pm 45^\circ$ with a source voltage of $\pm 1V$. If it's not a symmetric phase shift, further inspection and diagnosis of the problem should be done before moving on to the next steps. If everything checks out good, remove the source from the Phase CTRL input and proceed to the next step.
7. With the phase response flat, adjust R29 on the Phase Shifter Board to adjust the phase shift through the chassis. The phase response should be able to be adjusted down to 0° ($\pm 2^\circ$) over the 37MHz-53MHz bandwidth. It may take several iterations of adjusting the electrical delay on the network analyzer and R29 adjustments to achieve a phase response centered around 0° at 53MHz over the bandwidth of interest in the Booster RF System.
8. Gain is calibrated for each chassis using a ramp from 0-10V with a RF input of -19dBm at 53MHz to achieve a peak RF envelope of $\sim 1.06V$. This corresponds to 10.5dBm of RF output, which will give a 1kW output from the Fermi Solid State Driver Amplifiers. The gains of the ZFL-1000VH vary from unit to unit, so gain cannot be used as a determining factor for calibration. Use an 8005B Pulse Generator for generating the ramp signal to be used for amplitude calibration of the LLRF Chassis, and use a TDS3034B oscilloscope to measure the ramp and also the RF output at J1 of the LLRF Chassis. The plot should look like Figure 1 at the end of this document. If gain adjustment is needed to get the RF amplitude to be on the yellow horizontal trace of Figure 1, adjust R8 on the Variable Gain Amplifier board to achieve this. Once R8 is adjusted to match the plot in Figure 1, disconnect the ramp signal from the rear panel of the LLRF Chassis and measure Pin 6 of U6 on the Variable Gain Amplifier. If it does not read 0V, adjust R15 on the Variable Gain Amplifier until it does. Make sure that the RF output tracks the ramp in a linear fashion, and the RF output should be touching or slightly above the yellow horizontal trace on Figure 1. Note the delta of 10.5V on the scope. If there is a large deviation from the ramp response, the mixer in the Variable Gain Amplifier may need to be replaced. Save a plot of the ramp transfer function from the oscilloscope.

9. Once the gain and phase response has been adjusted, tune the electrical delay to a nominal 41ns by cutting the RG188 cable that goes from the output of the Mini-Circuits ZFL-2000+ Amplifier and the PD-40-100 4-way splitter. Typical delay for RG188: 0.12ns = 1 in. If the nominal delay cannot be reached by trimming this cable shorter, the RF input cable may be trimmed down to achieve the nominal electrical delay of 41 ns.
10. Save or print Bode plots of the S-parameters for each chassis for documentation purposes. Make a plot for each of the phase control voltages, -1V, 0V, and +1V.
11. Verify that the Program Inhibit works by putting in a +5V DC source into the Program Inhibit spigot on the rear panel of the chassis. RF should be significantly attenuated as shown on the network analyzer, and the red LED should illuminate on the front panel.
12. This completes the checkout and calibration procedure for the Booster LLRF chassis.

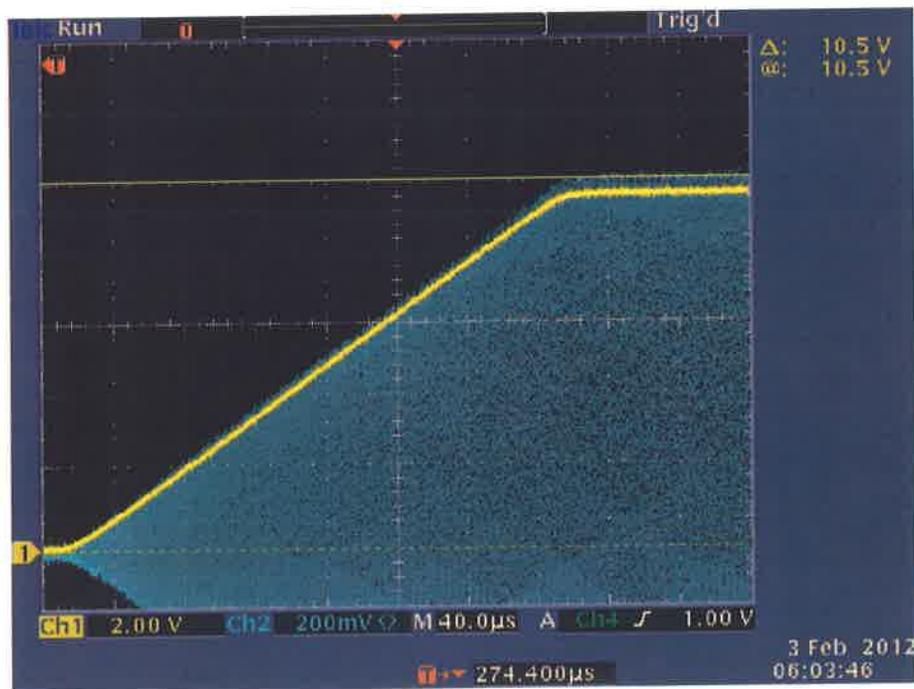


Figure 1. Typical Ramp Response of LLRF Chassis for 0-10V ramp.

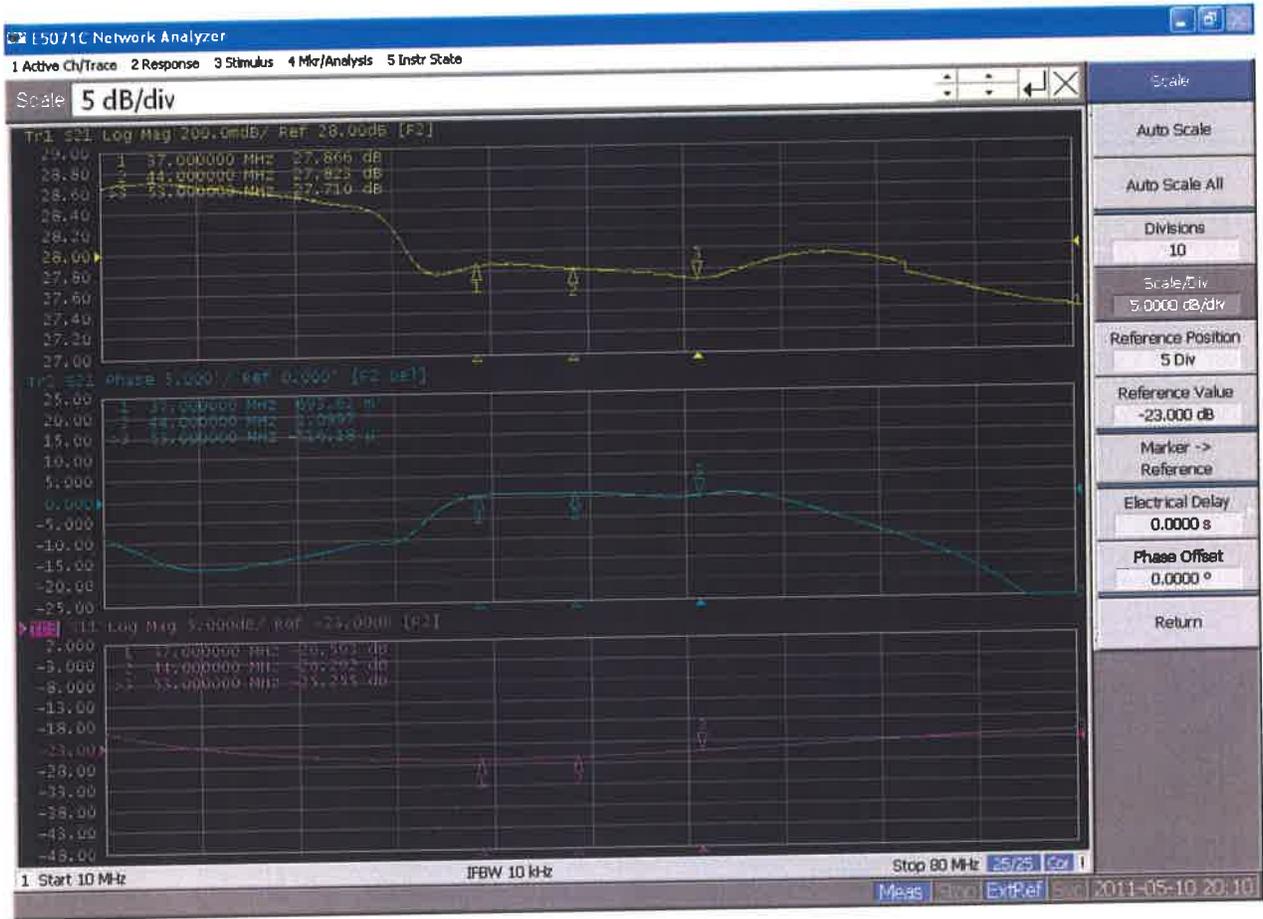


Figure 2. Typical Network Analyzer S parameter measurement at 0V phase control.

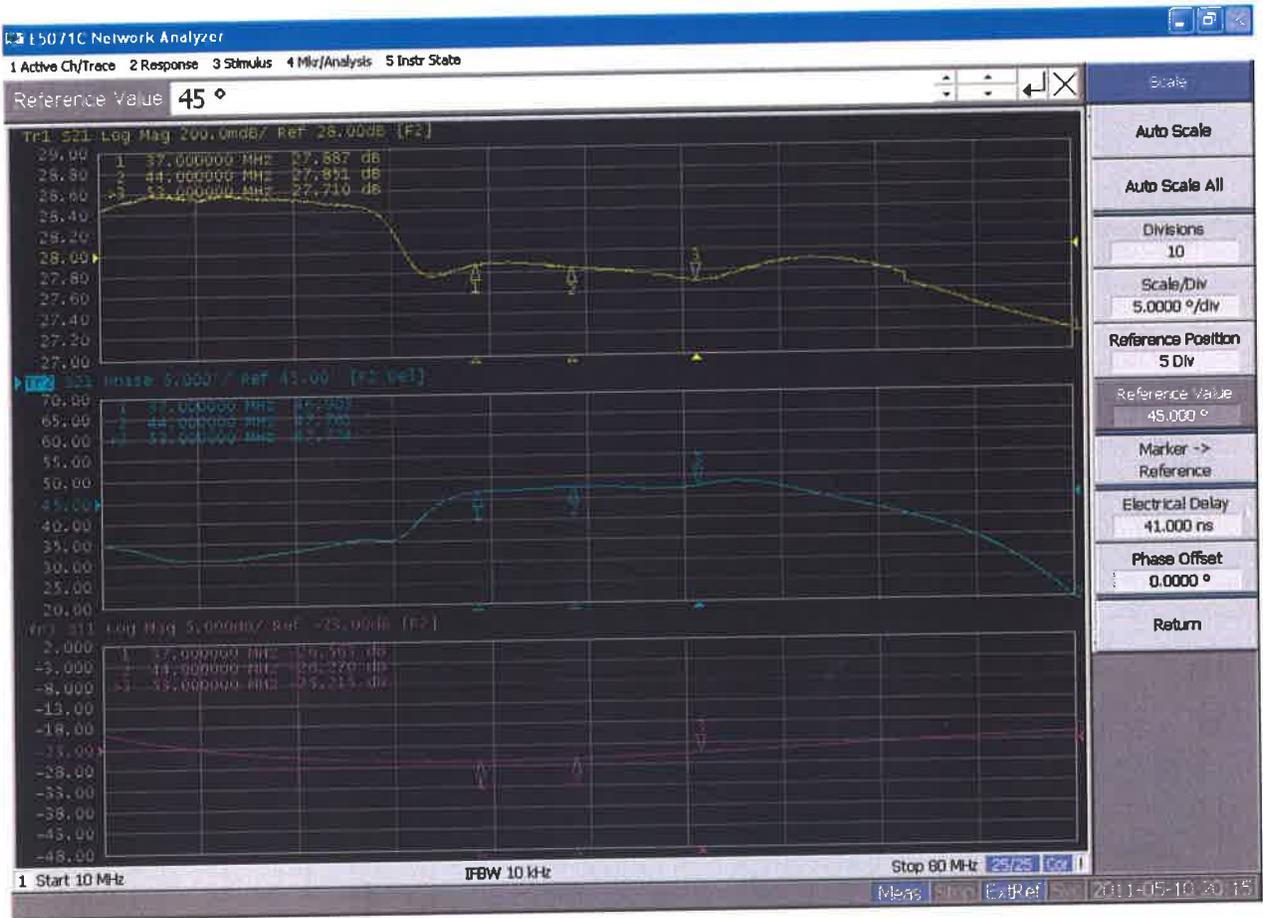


Figure 3. Typical Network Analyzer S parameter measurement at +1V phase control.

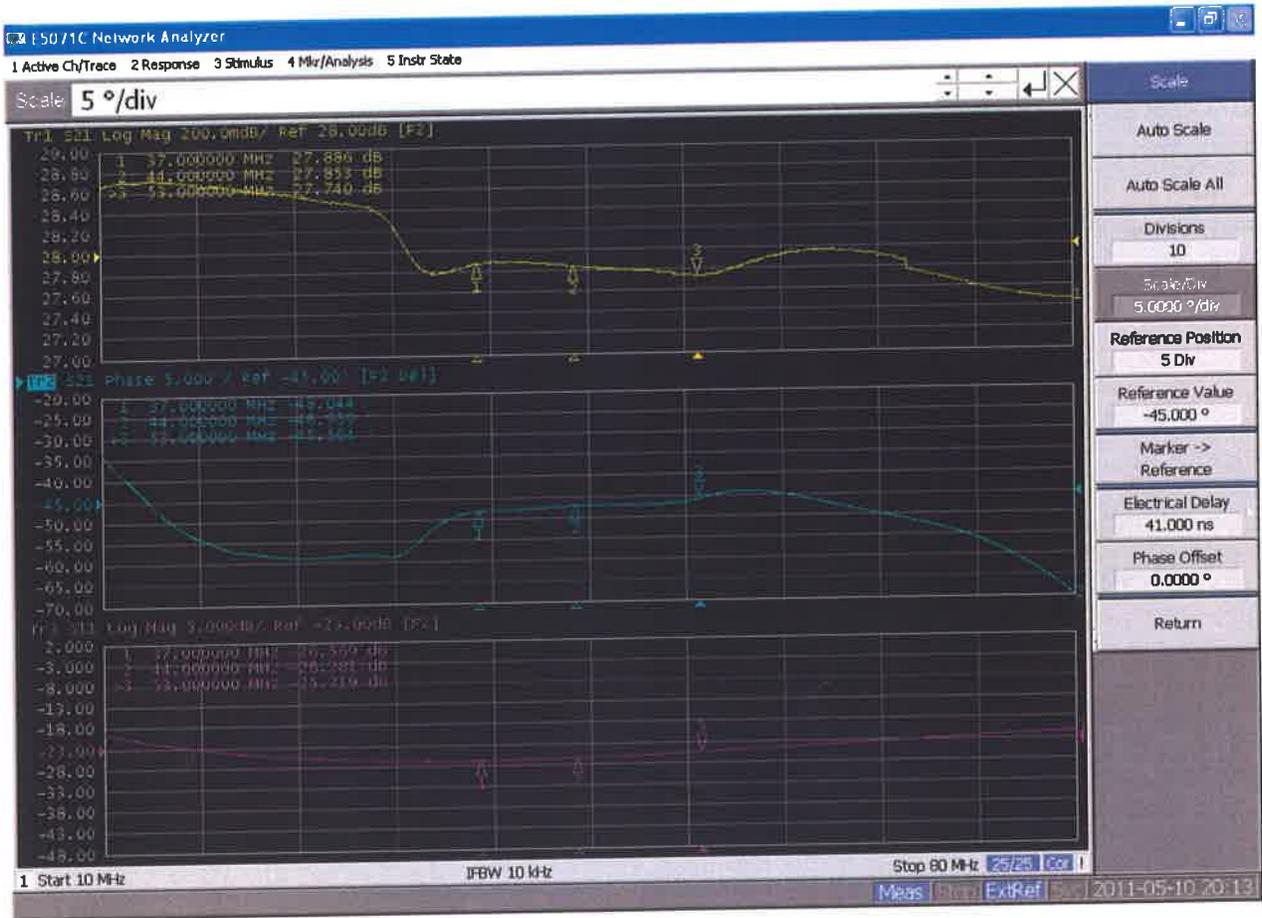


Figure 4. Typical Network Analyzer S parameter measurement at -1V phase control.