

## Waveform Generator/Sequencer Module

FNAL drawing 0230.00-ED-60650 (2-sheets)

### Section 1

#### Description In Brief.

The waveform generator and timing sequencer provide:

1. Start and stop pulses for the RF driver.
2. Gating signal for the low level RF mixer
3. Gradient/modulator program waveforms.
4. Crowbar compare pulse that changes the current trip point of the modulator H.V.P.S.

The outputs are found on the back of the A5 nim crate.

No output should exceed 500 micro-seconds in duration.

The sequence begins after receiving a positive start pulse, with a high level on the interlock enable input.

After a variable delay (mod start) the driver start pulse and the mixer gate pulse appear at their outputs at the same time. The driver start pulse lasts for 2.5 micro-seconds and the mixer gate pulse lasts until the driver stop pulse appears at its output.

After a delay of 8.5 micro-seconds, the external pulse interlock chassis determines if the driver output is at the proper level and if so, pulse interlock chassis will supply a high to the waveform generator enable input and the timing sequence will continue, thus starting the gradient waveform.

If the external pulse interlock chassis has not detected the proper driver level in 8.5 micro-seconds it will provide a low at the waveform generator enable input and will block the start of the gradient waveform. The driver stop pulse will be provided by the internal secondary timer 500 micro-seconds later.

After the gradient waveform has started, its duration can be adjusted from 200 micro-seconds to 500 micro-seconds by adjusting mod stop.

At the same timer, the crowbar compare signal will appear at the output and last the duration of the gradient.

After the gradient waveform has finished, the crowbar compare signal also terminates.

After a variable time delay (driver stop), the driver stop signal appears at its output for 2.5 micro-seconds, the mixer gate terminates its output at this time, and cycle is completed.

## Section 2

### Front Panel Description.

1. The waveform select knob will select one of 10 different pre-programmed waveforms that will control the gradient in the Linac RF tanks and minimize the reverse power reflected back on the 9 inch transmission line from the tank.
2. The tilt switch affects only the flattop portion of the gradient waveform. It allows flattop to tilt upward or downward. This switch is not normally used. Its original intention was to compensate for the droop in H.V.P.S. but the gradient regulator and modulator regulator have high enough gains to compensate for the droop in the H.V.P.S.
3. The mod start adjustment adjusts the start of the modulator referenced to the RF system start. It is normally used to center the entire gradient waveform on

the oscilloscope. It has a range from 5 to 75 micro-seconds.

4. The mod stop adjustment determines when the modulator waveform will stop. This will be the modulator pulse width control.
5. Driver stop adjustment determines how soon the driver will turn off after the modulator waveform stops. The driver stop pulse tracks the mod stop adjustment to prevent the modulator pulse width from being longer than the driver pulse width and also alleviates necessity the re-adjust driver stop when mod stop is adjusted.
6. The system start LED indicates that the start pulse appears at the input to the module and will go off entirely if the reset/off push button is in the off position.
7. The driver start LED indicates that the driver start pulse has appeared at the output module.
8. The c'bar compare (crowbar compare) LED indicates that the crowbar compare signal has started and appeared at the output of the module.
9. The interlock LED indicates that the pulse interlock chassis has prevented the sequencer from starting. Usually a D.C. condition (i.e. water, doors, mod ready, etc.) will stop sequencer from starting. If this LED appears, driver start, mod start, c'bar compare LED's will go out.
10. The mod block LED indicates that the waveform generator pulse has been terminated during its normal pulse width. Usually the pulse interlock module will stop the waveform generator if the driver RF has not reached the proper level in 8.5 micro-seconds or that the driver level has dropped too low during the normal driver pulse width, in which case will terminate the waveform generator during

its pulse width. If this LED appears, mod start and c'bar compare LEDs will go out.

11. The mod stop LED indicates an internal failure of the waveform generator/sequencer and will terminate and halt any further operation until the reset/off button is turned off, then turned back on again. Usually means that the waveform generator/sequencer has exceeded 500 microseconds as determined by an internal secondary timer. If this LED appears, the driver start, mod start, and c'bar compare LEDs will go out.
12. The power LED indicates that +5 volts is present in the module. It does not indicate + or - 15 volts.
13. The reset/off pushbutton will start or stop/reset the waveform generator/sequencer.

### Section 3

Circuit Description for the Waveform Generator/Sequencer.

- |      |   |
|------|---|
| U1A: | Monostable that drives the crowbar compare LED to on state for approximately 9.5 milli-seconds.                                     |
| U1B: | Not used.   |
| U2A: | Monostable that drives driver start LED to on state for approximately 9.5 mill-seconds.   |
| U2B: | Retriggerable monostable that goes low for 47 milliseconds to indicate on or off status of waveform generator/sequencer.            |
| U3A: | Not used.   |
| U3B: | Not used.   |
| U3C: | Looks at waveform generator enable and mod stop and if bad conditions exist will terminate the waveform output thru FET switch U38. |
| U3D: | Gates reset pulse to mod stop R-S flip-flop.  |

U4A: Not used.

U4B: Not used.

U4C: Input driver for Q1 providing driver stop pulse.

U4D: Input driver for Q4 crowbar compare pulse.

U4E: Input driver for Q3 providing on/off status of module to computer.

U4F: Input driver for Q2 providing driver stop pulse.

U5A: Part of the secondary timer that limits operation to 500 micro-seconds. Its output pulse triggers mod stop flip-flop if waveform generator fails.

U5B: Provides secondary driver off pulse in case waveform generator fails.

U6A: Gates either the waveform generator finish or secondary timer to terminate the crowbar compare signal (U11A-U11B).

U6B: Will allow the secondary timer pulse to get thru to the mod stop flip-flop (U6C-U6D) if the crowbar compare signal is too long.

U7A: 500 micro-second secondary timer that provides stop pulses if the waveform generator fails, also determines the window time of the module

U7B: Provides 2.5 micro-second driver stop pulse.

U8A/U8B: Both gates used as R-S flip-flop to form the mixer gate enable signal.

U8C: Used as inverter for driver stop buffer.

U8D: Gates both driver stop pulses coming from waveform generator (u7B) or secondary timer (U5B) two off pulses will appear at driver stop.

U9A: Monostable that produces 47 milli-second lockout to prevent double pulsing.

U9B: Monostable that drives system start LED to on state for approximately 9.5 milli-seconds.

U10A: Monostable that produces the driver on pulse width.

U10B: Variable monostable that delays turn on of sequencer from 5 to 75 micro-seconds (mod start).

U11A/U11B: Gates that are used as R-S flip-flop that from crowbar compare signal

U11C: Not used.

U11D: Part of the double pulse lockout circuit. It gates the RF start pulse, then is held off by U9A for 47 milli-seconds before allowing another pulse to get through.

U12A/U12B: Part of the delay circuit that hold the waveform generator off while the pulse interlock chassis checks for the proper driver level from the driver.

U13A/U13B: Double inverter to drive the interlock LED.

U13C: Inverts reset pulses to the mod stop flip-flop (U6C-U6D).

U13D: Inverts waveform enable signal to U18.

U13F: Not used.

U14: Latch that drives mod block light. It receives two strobe pulses, one at mod start time, the other when the waveform generator is finished, to determine if the waveform generator enable had remained high thru the entire waveform cycle.

Mod Block LED will be on if:

1. The waveform generator enable was not high at the time of mod start.

2. If the waveform generator enable did not remain high during the entire sequence cycle. This circuit is a latch and will not be reset until the next proper pulse sequence, therefore, the mod block LED may remain on even though the module has been placed in the off mode by the pushbutton.

- U15: Is a binary to decimal decoder that drives the waveform generators mode of operation (i.e. start, ramp up, flattop, ramp down, mod stop (finish)). See section six.
- U16: Is a binary step counter that selects what mode the waveform generator is in.
- U17A: Gate used as inverter to drive flattop counters in count up or down mode.
- U17B: Inputs signals will advance mode control counter, ramp up, flattop, ramp down, mod stop (finish).
- U17C: Inverter to drive the ramp clocks in waveform generator (U24-U25).
- U17D: Determines ramp up or ramp down mode of ramp clocks (U24-U25) in waveform generator.
- U18: Not used.
- U19: Produces mod start pulse for waveform generator.
- U20: Produces 9.5 milli-second pulse to drive mod start LED.
- U21A: Not used.
- U21B: Produces delay pulse to strobe EPROM latch 450 nano-seconds after the ramp counter has incremented/decremented one pulse. This monostable provides latching delay because the EPROM outputs are unstable for 350 non0seconds after an input change.
- U22: Not used.

- U23A: Programmable array logic (PAL) used as exclusive nor gate. It detects all highs or all lows on the input and gives a state change in output. Used on ramp up/down counters to establish when that part of the cycle is complete.
- U23B: Programmable array logic (PAL) used as exclusive nor gate. It detects all highs or all lows on the input and gives a state change in output. Used on flattop counters to establish when that part of the cycle is complete.
- U24/U25: Up/down counters used to control ramp up and ramp down of waveform generator. Output goes to EPROM to clock thru program.
- U26: Binary counter used as a clock divider. 16 MHz clock is used and output of this binary counter is 2 MHz.
- U27/U28: Up/down counter used to control tilt of the flattop portion of the waveform. At the end of the modulator stop (finish), one half value is loaded into these counters and they will count up or down from the  $\frac{1}{2}$  value.
- U29: EPROM that contains 10 separate pre-programmed waveforms that are selected from the front panel selector. The outputs of the EPROM drive a D/A converter that produces the actual waveform signal.
- U30: Latch that is used on the output of the EPROM because the EPROM is unstable for 350 nano-seconds after input change, the latch is strobed 450 nano-seconds after U21B.
- U31: VCO clock that drives the tilt counters. Its speed actually controls the flattop pulse width (Mod stop control).
- U32: D/A converter that actually produces the flattop tilt. Output is summed into U33 and becomes

reference for U34. Input is controlled by up/down counters U28-U27.

- U33: Op-27 op am that adds reference signal and tilt signal from U32 D/A and its output goes to ramp D/A U34.
- U34: D/A converter that actually produces the ramp up and ramp down signals that produce the modulator/gradient waveform.
- U35: Op amp used as a buffer for the ramp D/A (U34). Its output goes thru switch (U38) to become the gradient program.
- U36: Monostable that produces a pulse whenever ramp down is finished (used to advance waveform mode counter U16).
- U37: Monostable that produces a pulse whenever tilt up or tilt down is finished (used to advance the waveform mode counter U16).
- U38: FET switch that's used as a SPDT switch. It cuts off the gradient program in the event of the waveform generator enable input goes low.

#### Setup Instructions For Waveform Generator.

Note: It would be convenient to use test fixture but not necessary.

1. Apply power to the module, power LED should light.
2. Provide +5 volts on the sequencer enable input waveform generator input.
3. Provide a start pulse, +5 volts, 5 micro-seconds pulse width, at a 15 Hz rate.

4. Outputs should be terminated in 50 ohms:
  - a. Driver start output.
  - b. Driver stop output.
  - c. Crowbar compare output.
5. Outputs that should not be terminated:
  - a. Gradient waveform output.
  - b. Mixer gate output.
6. Turn front panel controls fully counter clockwise. Tilt switch to center (no tilt). Turn waveform selector switch to zero position.
7. Push the off/reset button to on state.
  - a. The pushbutton LED should light continuous.
  - b. System start LED will pulse.
  - c. Driver start LED will pulse.
  - d. Mod start LED will pulse.
  - e. C'bar compare LED will pulse.
  - f. Interlock LED should be out.
  - g. Mod block Led should be out.
  - h. Mod stop LED should be out.
  - i. Power LED should remain on.
8. If step six is o.k., continue this checkout list. If step six is not o.k., refer to circuit description section.
9. Check module output against the timing chart.

## Section 5

The 2732A EPROM Programming and Readout Description and Theory of Operation.

The 2632 EPROM is a 23k memory arranged in a 10x256x8 bit pattern. In the future, this could be expanded to its full capability of 16x256x8 but it isn't needed presently.

The memory contents only contain the leading edge of the waveform selected. From the starting location, the memory address is incremented 256 steps, producing the leading edge of the waveform. The trailing edge of the waveform is produced by decrementing the memory address 256 steps back to the starting location.

The waveform selector knob on the front panel of the waveform generator selects which block of memory will be used. The output of the memory contains a digital representation of magnitude that is fed to a digital to analog converter that produces the actual waveform output.

## Section 6

Explanation of the Operating of the Waveform generator Section.

The heart of the waveform generator is the mode selector, (U15-U16), that controls the four modes of the waveform generator.

They are:

1. 0 state = ramp up mode.
2. 1 state = flat top mode (up, down, or off).
3. 2 state = ramp down mode.
4. 3 state = reset/finish mode.

The pulse sequencer supplies the start pulse that zeros (U15-U16), a counter and decimal decoder, which acts as the mode selector.

The mode selector is now in the zero state which is the ramp up mode.

The mode selector puts ramp counters, (U24-U25), in a count up mode and also gates the clock that feeds the ramp counters.

The ramp counters (U24-U25) increment from zero up to 256 counts, that step the 32 k EPROM (U29) up through its program. The EPROM output goes thru a latch (U30) and reaches ramp D/A converter (U34) that actually produces the waveform.

A programmable array logic (PAL) (U23A) has been set up to act as an exclusive nor gate. The PAL detects when the output of the EPROM (U29) reaches full value, then triggers the mode selector (U15-U16). The mode selector stops the clock that feeds the ramp counters (U24-U25) that run the EPROM (U29).

The mode selector is now in the one state which is the tilt mode.

At this time, mode selector (U15-U16) enables the tile converters (U27-U28) that drive the tilt D.A converter (U32). The tile D/A converter (U32) will change the reference level applied to ramp D/A converter (U34), causing the waveform's flattop region to tilt upward, downward, or not at all, depending on the position of the tilt switch (S1) on the front of the panel.

The front panel switch causes the tilt counters (U27-U28) to either count up or down. The switch also controls the reference level applied to the tile D/A converter (U32). If the switch is in center position (no tilt), it removes the reference level applied to the tilt D/A converter (U34) so that D/A output will remain not changed even though the tilt counters (U27-U28) are running.

The tilt counters (U27-U28) must continue to clock to determine the width of the flattop. The width of the flattop is controlled by the variable clock (U31) that drives the tile counters (U27-U28).

U32B, exclusive nor gate PAL, detects when the tilt counters (U27-U28) reach maximum or zero value. The PAL supplies a trigger to the mode selector (U15-U16) which stops the tilt counters (U27-U28) and completes the tilt mode.

The mode selector is now in the two state which is ramp down mode.

At this time, mode selector (U15-U16) selects the count down mode for the ramp counter clock.

The ramp counters (U24-U25) decrement the EPROM (U29) back down thru the same program, thereby creating the trailing edge of the waveform. The exclusive nor gate PAL (U23A) detects when the EPROM output reaches zero value and triggers the mode selector (U15-U16). The ramp down mode is complete.

The mode selector (U15-U16) is now in the three state which is the reset/finish mode. At this time, the mode selector does four things:

1. Stops the clock that drives the ramp counters (U24-U25).
2. Clears the ramp counters (U24-U25).
3. Loads the  $\frac{1}{2}$  value into the tilt counters (U27-U28) so tilt counters count equally in either up tilt or down tilt mode.
4. Supplies the sequencer section with a logic level that indicates waveform is finished.

The cycle of the waveform generator is now complete.

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