

# Amplitude Control Module

## 1. Brief Description of the Amplitude Control Module:

The amplitude control module is a digital variable attenuator capable of 0 to -72 dB output. The user can select one of two inputs by connecting an external jumper wire.

One input is a fixed 10VDC voltage reference. The other is a low bandwidth video port (about 1 MHz bandwidth).

After the input has been selected it is sent to a digital to analog converter that acts as the variable attenuator.

The output from the D/A converter is fed thru a buffer amplifier to the output.

The amount of attenuation is selected by operating a simple counter whose output represents an order of magnitude. The counter output drives the D/A converter, thus adjusting the output.

The front panel knob controls the output. Center position is stop, counter-clockwise decreases value, clockwise increases value.

The front panel has a three digit readout which corresponds to the output in percent.

The pushbutton will instantly clear and zero the amplitude controller module output.

## 2. Detailed Description of the Amplitude Control Module:

Refer to FNAL dwg. 0230.00-ED-60643 (2 sheets).

Presently, the amplitude control module is used to adjust the output of the waveform generator and we will use this as the example.

The external input jumper has been selected and the input has a maximum value of +3 volts, which is fed to the reference input of the digital to analog converter (U17).

The attenuation is selected by running a simple counter whose output represents an order of magnitude, and is fed to the D/A converter.

There are three up/down counters, (U10-U11-U12) that are controlled by either a local clock (U24-U23-U11), or the computer which sends (CW) up or (CCW) down pulses to the amplitude control module input.

U1-U2-U3-U4-U8-U9 make up the clock gating circuits.

U3-U5-U6 make up the maximum-minimum clock bounds so that the output doesn't toggle over maximum or under minimum and cause the output to jump.

The output of the counters are fed to a digital to analog converter (U17) that acts as a variable attenuator. The input enters reference input, the output will be divided by 4096.

The output of the D/A is fed to a sample and hold (U16) that acts as a de-glitching circuit.

The sample and hold feeds a 50 ohm video buffer (U15) which drives the output.

The three digit front panel display and the maximum-minimum clock bounds are controlled by a 2716 Eprom. These two functions are multiplexed and are controlled by (U13), a timer set up as an oscillator. (U13) output toggles the Eprom's LSB, selects which display will be loaded, and triggers (U6A & B), a latch which controls the maximum-minimum boundaries of the counters (U10-U11-U12).

When the maximum counter value is reached, (U6A) stops the CW (up) pulses. When the minimum counter value is reached, (U6B) stops the CCW (down) pulses.

The numbers that are displayed on the 3 digit readout corresponds to the output in percent. The Eprom looks at the counter, then displays the number.

### 3. Circuit Description of the Amplitude Control Module:

- U1: Monostable that increases the input pulse to 12 milliseconds. It also has an input that shuts off the external clock if the internal clock is running. This gives the local operator precedence over the remote operator.
- U2A & B: Dual Monostable that multiplies the external clock by two, if desired. It will decrease the resolution from 4096 to 2048. If increased resolution is desired, pin 5 should be disconnected from pin 12.
- U3A: Used as an inverter, part of the readout decoder circuit.
- U3B: Recombines output from U2A & B and makes one remote clock output. (CCW-down).
- U3C: Recombines output from U9A & B and makes one remote clock output. (CW-up).
- U3D: Gate that enables (U6B) D-flip flop when the counters have two low LSB bits. If (U6B) detects a high from the Eprom, output will inhibit down clock.
- U4A: Inhibits up pulses from reaching counters if counters are at full value. Keeps counters from toggling over maximum to minimum value.
- U4B: Inhibits up pulses from reaching counters if counters are at minimum value. Keeps counters from passing thru minimum to maximum value.
- U4C: Gates either local clock or computer clock CW (up) pulses.
- U4D: Gates either local clock or computer clock CCW (down) pulses.
- U5A: Gate that enables (U6A) D-flip flop when the counters have two high LSB bits. If (U6B) detects a high from the Eprom, output will inhibit up clock.
- U5B: Used as an inverter.
- U5C: Gates up or down pulses to (U22A). Purpose is to strobe sample and hold (U16) after counters have incremented or decremented.

U5D: Gates either front panel clear or interlock enable. Purpose is to clear counters and zero the module output.

U6A: D-flip flop that controls the CW (up) clock that drive the counters. If a high is detected from the Eprom, when the counters are at maximum, the output of (U6A) inhibits the CW (up) clock. This keeps display and output from passing thru maximum to minimum.

U6B: D-flip flop that controls the CCW (down) clock that drive the counters. If a high is detected from the Eprom, when the counters are at zero, the output of (U6B) inhibits the CCW (down) clock. This keeps display and output from passing thru minimum to maximum.

U7: The binary decoder for the right digit.

U8: Monostable that increases the input pulse to 12 milliseconds. It also has an input that shuts off the external clock if the internal clock is running. This gives the local operator precedence over the remote operator

U9A & B: Dual Monostable that multiplies the external clock by two, if desired. It will decrease the resolution from 4096 to 2048. If increased resolution is desired, pin 5 should be disconnected from pin 12.

U10-U11-U12: Binary up/down counters that driver the analog to digital converter and Eprom display controller. The counter output represents the order of magnitude of the analog to digital converter output.

U13: Timer operating as a clock. The output is used to select a number from the Eprom and drive the proper display.

U14: Binary decoder driver for the middle digit.

U15: 50 ohm output driver.

U16: Sample and hold that de-glitches the output of the analog to digital converter. At the beginning of a clock pulse, a sample and hold receives a hold pulse from (U5C-U22) that locks to the last known value of the A/D. After hold returns to sample mode, and is

transparent. When A/D inputs are changing, the output is not stabilized. Sample and hold provides for a smooth transition.

U17: Analog to digital converter that acts as a variable attenuator. The input from the counters is an order of magnitude that controls the output of the D/A converter.

U18: 2716 Eprom that does four functions in two steps. (U13) NE555 has been set up as an oscillator that toggles the LSB input to the Eprom (pin 8).

Step one occurs when Eprom input pin 8 is high. This selects all of the even address outputs. The even address outputs contain a (percent) number that is loaded into the left display digit. It also contains the two bits that control the up/down clock feeding the counters.

When all of the Eprom inputs are high, Eprom output pin 14 supplies a high to (U6A) which will inhibit the CW (up) clock. When all of the Eprom inputs are low, the Eprom output bit 17 supplies a high to (U6B), which will inhibit the CCW (down) clock.

(U5A) enables (U6A) strobe so that a CW (up) clock inhibit only occurs at the absolute maximum counter value.

(U3D) enables (U6B) strobe so that a CCW (down) clock inhibit only occurs at the absolute minimum counter value.

At any counter value other than maximum or minimum count, Eprom output pins 14 and 17 are low so that if (U5A) or (U3D) enables the strobes to (U6A or B) the up or down clock pulses will not be inhibited.

Step two occurs when Eprom input pin 8 is low. This selects all of the odd address outputs. Odd address outputs contain a (percent) number that is loaded into the middle and right displays.

A review of the 2716 Eprom program listing would be helpful to understand the multiple functions of this device.

U19: Binary decoder driver for the left digit.

U20: +10VDC

U21A-B-C-D: Gates the up and down pulses from the local clock generator (see explanation of U23 and U24)

U22A: Monostable that supplies a 3 micro-second hold pulse to the sample and hold (U16) is triggered by either up or down pulses supplied by (U5C).

U22B: Re-triggerable monostable that triggers when local clock is running. Q output (pin 10) blocks the remote clock inputs. Q bar output (pin 9) gives the computer a low status that indicates the local clock is operating.

The retriggerable monostable has a 2 second output time lag after the last clock input

U23: Comparator that looks at the bridge circuit containing R1. When R1 is counter clockwise, U23 output is low, thus controlling U21 to produce CCW (down) pulses. When R1 is clockwise, U23 output is high, thus controlling U21 to produce CW (up) pulses.

U24: Timer that is set up as a variable speed oscillator. R1 controls the threshold voltage of the timer, therefore controlling the duty cycle. In the center position, R1 supplies a voltage to the threshold input that is too low. The time output stops.

As the slider of R1 is moved away from center, the threshold voltage is exceeded and the timer begins timing a long duty cycle. The output speed of the timer is slow.

As the slider is moved farther away from center, the threshold is exceeded much sooner, thus the speed of the output is increased.

The center dead band region of R1 is adjusted by R35.

#### 4. Setup instructions for the Amplitude Control Module:

Note: It would be convenient to use the test fixture although it is not necessary.

1. Turn front panel control knob fully counter clockwise.
2. Apply power to the module. At this time, the display should read (.0) or a random number may appear on the display. If a number is present, it should decrement until it read (.0) and should stop there.

Note: If the display decrements thru (.0) and jumps to (99.9) and continues to decrement, check U3-U4-U5-U6-U13-U18.

3. With the display at (.0), turn control knob fully clockwise. The display should increment until it displays (99.9) and should stop there.

Note: If display increments thru (99.9) and jumps to (.0) and continues to increment, check U3-U4-U5-U6-U13-U18.

Note: If display refuses to increment, check U23-U24 and/or adjust R35

4. Turn control knob counter clockwise. Display should decrement. When display reads about (50.0), turn control knob to center range. This should stop display.

Note: If display cannot be stopped, adjust R35.

5. With control knob in center ranger, adjust R35 for a plus and minus 30 degree dead band.
6. Set display for about (50.0) and press the front panel reset button. Display should read (.0).
7. Apply a pulse to the input, +3 volts. If the display reads (.0), there should be no output.
8. Turn the control knob clockwise to increment the display. Output should increase in amplitude until display reads (99.9). The output should equal the input.

9. Push front panel reset button. Display should read (.0) and output should go to zero.

10. Remove the pulse input. Short input to ground. The output should be zero, plus or minus a few millivolts.

If it is not, adjust R36 (offset adj.) for zero output.

## 5. The 2716 Eprom Readout Explanation:

The 2716 Eprom does four functions in two steps.

In the even addresses, information for the clock bound and left digit are contained.

The first half byte contains the clock bound instructions. They are:

1. E = inhibit the CCW (down) clock.
2. 0 = permit either CCW (down) or CW (up) clock.
3. 7 = inhibit the CW (up) clock.

The second half byte contains the left digit display number. It reads out directly. If this half byte contains an (F), the display will blank out. This is used only to blank the leading zeros.

In the odd addresses, information for the middle and right digit is contained.

The first half byte contains the middle digit display number. It reads out directly. If this half byte contains an (F), the display will blank out. This is used only to blank the leading zeros.

The second half byte contains the right digit display number. It reads out directly. This half byte will never display an (F).

LW:nf